SPECIFICATION

Graphic Type STN Dot Matrix LCD Module

JM12032A

Kentec GmbH - Elektronische Bauelemente - www.kentec.net

GENERAL SPECIFICATION

128 X 64 dots display
New JRC LCD driver:NJU6450A
Interface with 8-bit MPU (directly connected to M6800 serial MPU)

Display Specification

Display dot: 120 X 32

Display type: STN and FSTN

Display color-Display background color: Yellow-Green,Blue-Gray, Black-White

Polarizer mode: Positive,Negative;Reflective ,Transflective,Transmissive

Viewing angle: 6:00 and 12:00

Display duty: 1/32

Driving bias: 1/7

Display RAM: 5120 bits

Mechanical characteristics (Unit:mm)

External dimension: 98.0 X 50.0 X 10.0 (15.0 for LED Backlight)

View area: 76.0 X 25.2

Dot size: 0.55 X 0.61

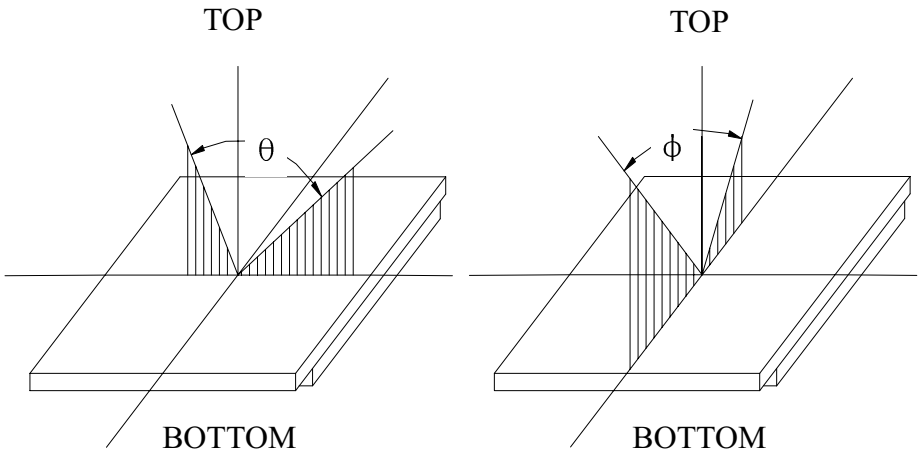
Dot pitch: 0.60 X 0.66

Weight: 86g (115g for LED backlight)

POWER: negative power，+5V power

● Optical Characteristics

(1) Definition of viewing Angle



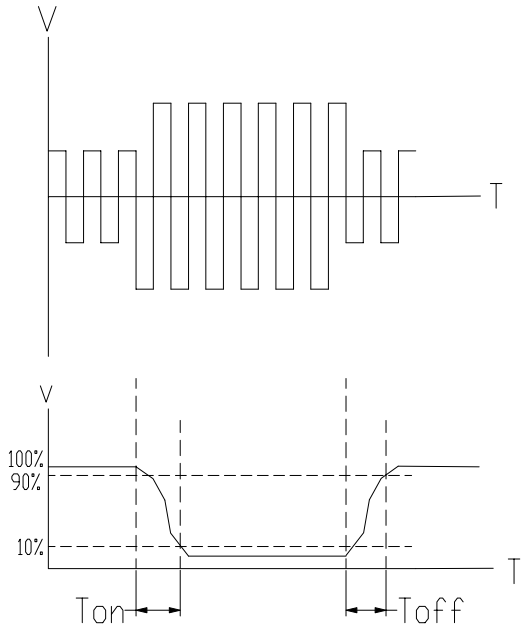
(2) Definition of Contrast Ratio:

$$\text{Contrast Ratio} = \frac{\text{Reflectance value of non-selected state brightness}}{\text{Reflectance value of selected state brightness}}$$

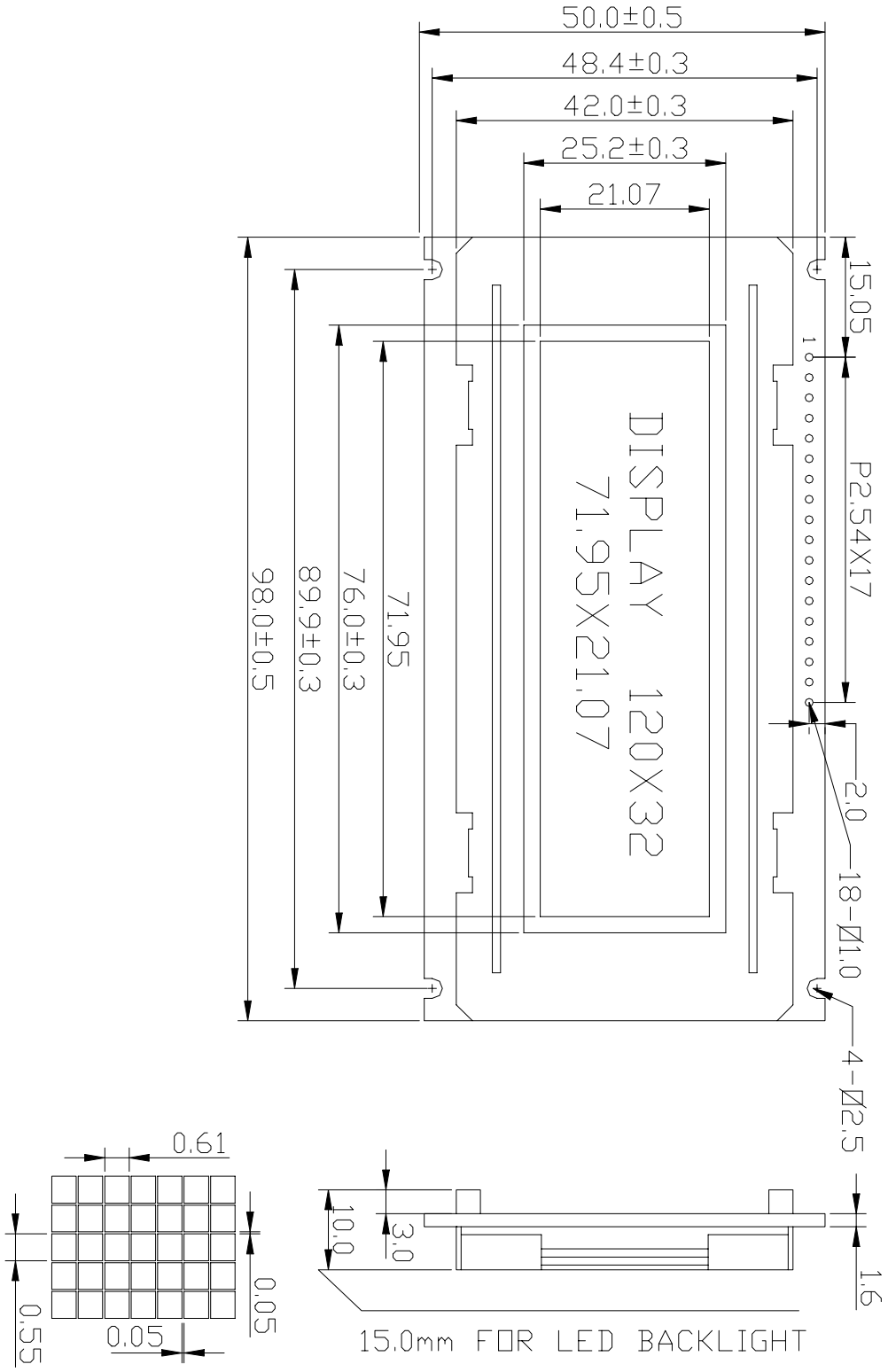
Test condition : standard A light source

(3) Response Time

Response time is measured as the shortest period of time possible between the change in state of an LCD segment as demonstrated below



● External Dimension



● Absolute Maximum Ratings

Item	Symbol	Condition	Standard Value		Unit
			Min	Max	
Supply Voltage for logic	Vdd	Ta=25℃	-0.3	7.0	V
Supply Voltage for LCD	Vee		Vdd-13.5	0	V
Input Voltage	Vr		-0.3	Vdd+0.3	V
Operating Temperature	Top	-	0	50	℃
Storage Temperature	Tstg	-	-20	70	℃

● Electrical Characteristics (Ta=25℃, Vdd= 5.0V)

Item	Symbol	Condition	Standard Value			Unit
			Min	Type	Max	
Supply Voltage for logic	Vdd-Vss	-	4.5	5.0	5.5	V
Supply Current for logic	Idd	Vdd=5.0	-	1.47	-	mA
Driving Current for LCD	Iee	Vee=-4.2	-	1.46	-	mA
Driving Voltage for LCD	Vdd-Vee	-	-	9.2	-	V
Input Voltage H level	V_{IH}	H	0.8Vdd	-	Vdd	V
Input Voltage L level	V_{IL}	L	Vss	-	0.8	V

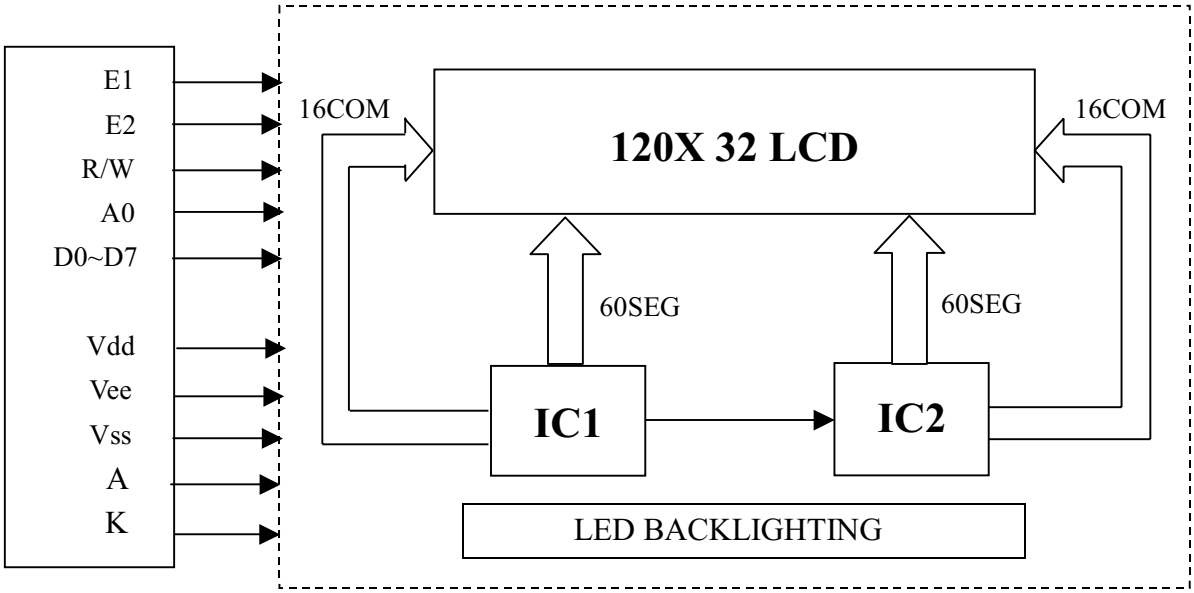
● Absolute Maximum Ratings For LED Backlight

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
LED Forward Consumption Current	If	Ta=25℃ Vf=4.1V	-	210	-	mA
LED Allowable Dissipation	Pd	-	-	880	-	mW

● Pin assignment

Pin NO.	Symbol	Function		Remark
1	Vss	Power supply	0V	
2	Vdd		+5V	
3	Vee		For LCD	Variable
4	A0	Register select H:data L:instruction		
5	R/W	read/write		
6	E1	IC1 enable		
7	E2	IC2 enable		
8	NC	No connection		
9	D0	Data bus bit 0		
10	D1	Data bus bit 1		
11	D2	Data bus bit 2		
12	D3	Data bus bit 3		
13	D4	Data bus bit 4		
14	D5	Data bus bit 5		
15	D6	Data bus bit 6		
16	D7	Data bus bit 7		
17	A	Anode of LED Unit		
18	K	Cathode of LED Unit		

● Block Diagram

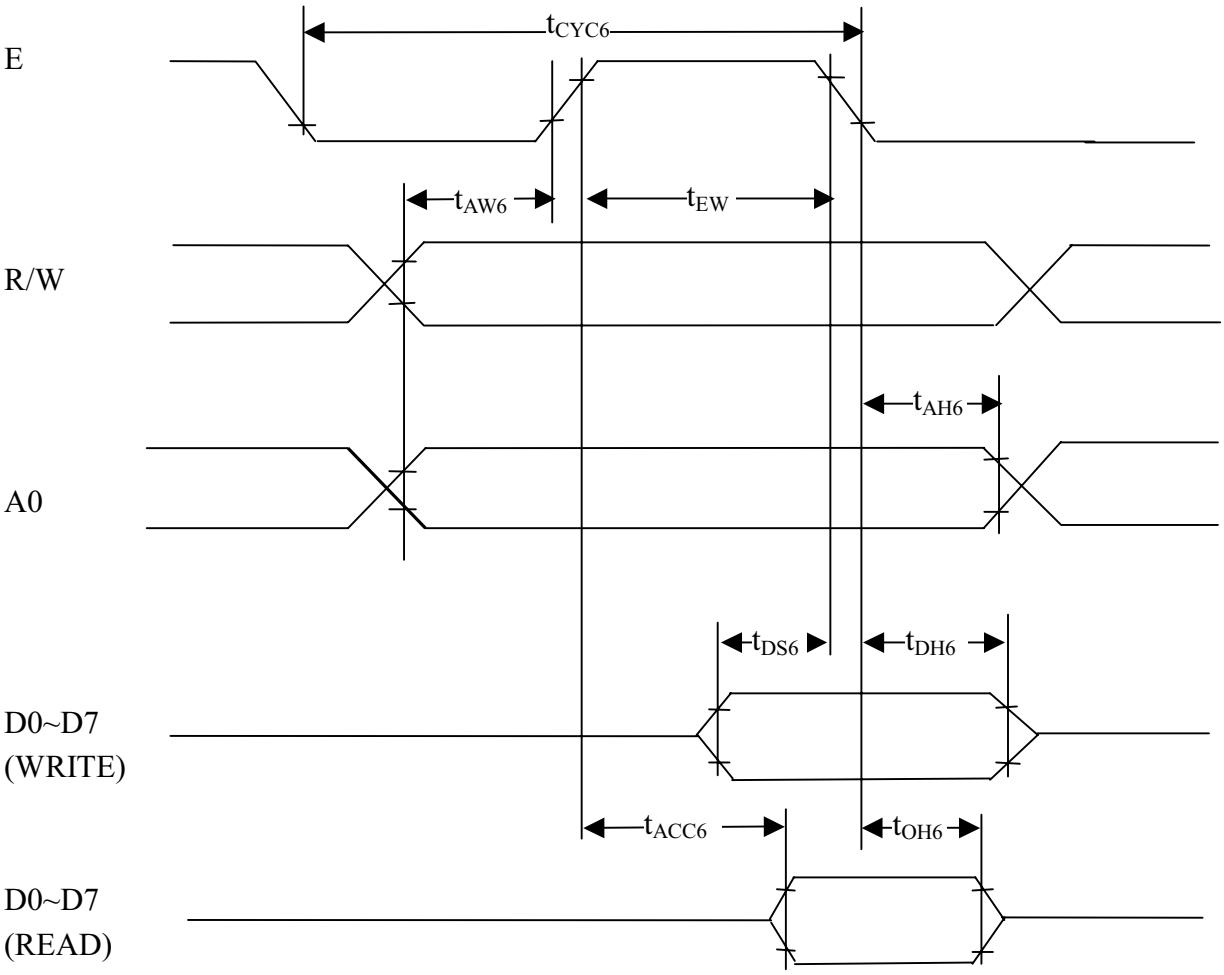


● MPU Interface

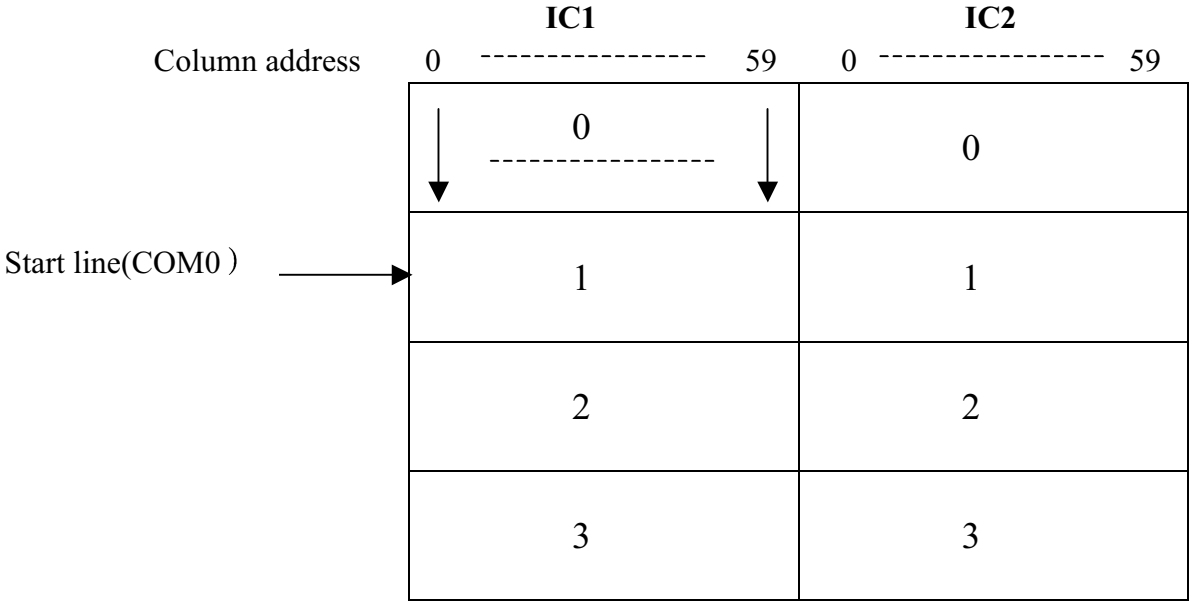
（V_{DD}=5.0V ± 10%,V_{SS}=0V,T_a=-20~+75℃）

Parameter		Symbol	Min	Max	Condition	Unit
Address set up time		t_{AW6}	20			ns
Address hold time		t_{AH6}	10			ns
System cycle time		t_{CYC6}	1000			ns
E pulse width	Read	t_{EW}	100			ns
	Write		80			ns
Data set up time		t_{DS6}	80			ns
Data hold time		t_{DH6}	10			ns
Access time		t_{ACC6}		90	C_L=100pF	ns
Output disable time		t_{OH6}	10	60		ns

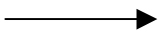
*Input signal rise time and fall time are less than 15ns.



● Reflector of Screen and Display RAM



Correspondence with arrow direction and BIT:



Column adress	ADC	D0=0	00	01	02	03	04	05	06	----------→	4F
		D0=1	4F	4E	4D	4C	4B	4A	49	←----------	00
SEG Term.			0	1	2	3	4	5	6	------- 60 ------	79

● Instruction code

Instruction	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Description
Display on/off	0	0	1	0	1	0	1	1	1	0/1	Whole disp on/off 1:on 0:off
Display start line	0	0	1	1	0	Display start address (1~31)					Determine the disp line correspond to the COM0
Page address set	0	0	1	0	1	1	1	0	Page (0~3)		Set the page of disp data RAM
Column address set	0	0	0	Column address (0~79)							Set the column address of disp data RAM
Status read	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0	BUSY 0:ready 1:working ADC 0:counterclockwise 1:clockwise output ON/OFF 0:disp on 1:disp off RESET 0:normal 1:reset
Write display data	1	0	Write data								Write data to disp RAM / Access the predetermied address of the disp RAM
Read display data	1	1	Read data								Read data from disp RAM
ADC select	0	0	1	0	1	0	0	0	0	0/1	Determine the mode reading of the disp RAM 0:clockwise output 1:counterclockwise output
Static drive on/off	0	0	1	0	1	0	0	1	0	0/1	Select the dynamic or static driving 1:static driving 0:dynamic driving
Duty ratio select	0	0	1	0	1	0	1	0	0	0/1	Select the duty ratio 0: 1/16 1: 1/32
Read Modify write	0	0	1	1	1	0	0	0	0	0	Increment the column address register when writing but no change when reading
END	0	0	1	1	1	0	1	1	1	0	Release from the Read Modify Write mode
Reset	0	0	1	1	1	0	0	0	1	0	Set the display start line register to 1st line,page add. Register to 3
Power save (dual command)	0 0	0 0	1 1	0 0	1 1	0 0	1 0	1 1	1 0	0 1	Set the power save mode by selecting disp off and static driving on

● Instruction Description

A. Display On/Off

This is instruction executes whole display On/Off no relation with the data in the Display Data RAM and internal conditions.

	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	0	1	0	1	0	1	1	1	D

D 0: Display On
1: Display Off

When the static driving mode is selected (static drive On) in display Off status, the internal circuits put on the power save mode.

B. Display Start Line

This instruction set the line address. The selected line in the Display Data RAM correspond to the COM0 Which display at the top of LCD panel.
The display area is set automatically from the selected line to the line which increased the number of duty ratio.
Therefore, the smooth scroll for vertical direction by changing the start line address one by one or page switching are available by this instruction.

	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	0	1	1	0	A4	A3	A2	A1	A0

A4	A3	A2	A1	A0	Line Address
0	0	0	0	0	0
				1	1
1	1	1	1	0	1E
1	1	1	1	1	1F

C. Page Address Set

When MPU access the display Data RAM, the page address corresponded to the row address must be selected.
The access in the display Data RAM is available by setting the page and column address.
The display is no change when the page address is changed.

	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	0	1	0	1	1	1	0	A1	A0

A1	A0	Page
0	0	0
0	1	1
1	0	2
1	1	3

D. Column Address Set

This instruction set the column address in the Display Data RAM.
When the MPU access the Display Data RAM continuously, the column address increase"1" automatically, therefore, the MPU can access the data only without address setting.
The increment of the column address is stopped by the address of 50H automatically, but the page address is no change even if the column address increase to 50H and stop.

	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	0	0	A6	A5	A4	A3	A2	A1	A0

A6	A5	A4	A3	A2	A1	A0	Column Add.
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
1	0	0	1	1	1	0	4E
1	0	0	1	1	1	1	4F

E. Status Read

This instruction read out the internal status.

	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY: BUSY=1 indicate the operating or the Reset cycle.
The instruction can be input after the BUSY status change to “0”.

ADC: Indicate the output correspondence of column(segment)address and segment driver.
0: Counter clockwise Output (Inverse)
Column Address 79-n ←——→ Segment Driver n
1: Clockwise Output (Normal)
Column Address n ←——→ Segment Driver n

ON/OFF: Indicate the whole display On/Off status.
0: Whole Display ”On”
1: Whole Display ”Off”
(**Note**) The data ”0=On” and “1=Off” of Display On/Off status read out is inverted with the Display On/Off instruction data of “1=On” and “0=Off”.

RESET: Indicate the initialization period by reset instruction.
0: ——
1: Initialization Period

F. Write Display Data

This instruction write the 8-bit data on the data bus into the Display RAM.
The column (segment) address increase “1” automatically when writing, therefore, the MPU can write the 8-bit data into the Display Data RAM without address setting.

	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Code	1	0	Write Data							

G. Read Display Data

This instruction read out the 8-bit data from Display Data RAM which addressed by the column and page address. In case of the Read Modify Write Mode is Off, the column address increase "1" automatically after each read out, therefore, the MPU can read out the 8-bit data from the Display Data RAM continuously without address setting.

A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1	1	Read Data							

H. ADC Select

This instruction set the correspondence of column address in the Display Data RAM and segment driver out. Therefore, the order of segment output can be changed by the software, and no restriction of the LSI placement against the LCD panel.

	AO	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	0	1	0	1	0	0	0	0	D

D 0: Clockwise Output (Inverse)
1: Counter Clockwise Output (Normal)

I. Static Drive On/Off

This instruction executes the all common output terns on and whole display on obligatory.

	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	0	1	0	1	0	0	1	0	D

D 0: Static Drive Off (Normal Operation)
1: Static Drive On (Whole Display Turns On)

When the Display Off mode is selected (Display Off) in Static Driver On status, the internal circuits put on the power save mode.

J. Duty Select

This instruction set the LCD driving duty ratio.

	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	0	1	0	1	0	1	0	0	D

D 0: 1/16 duty
1: 1/32 duty

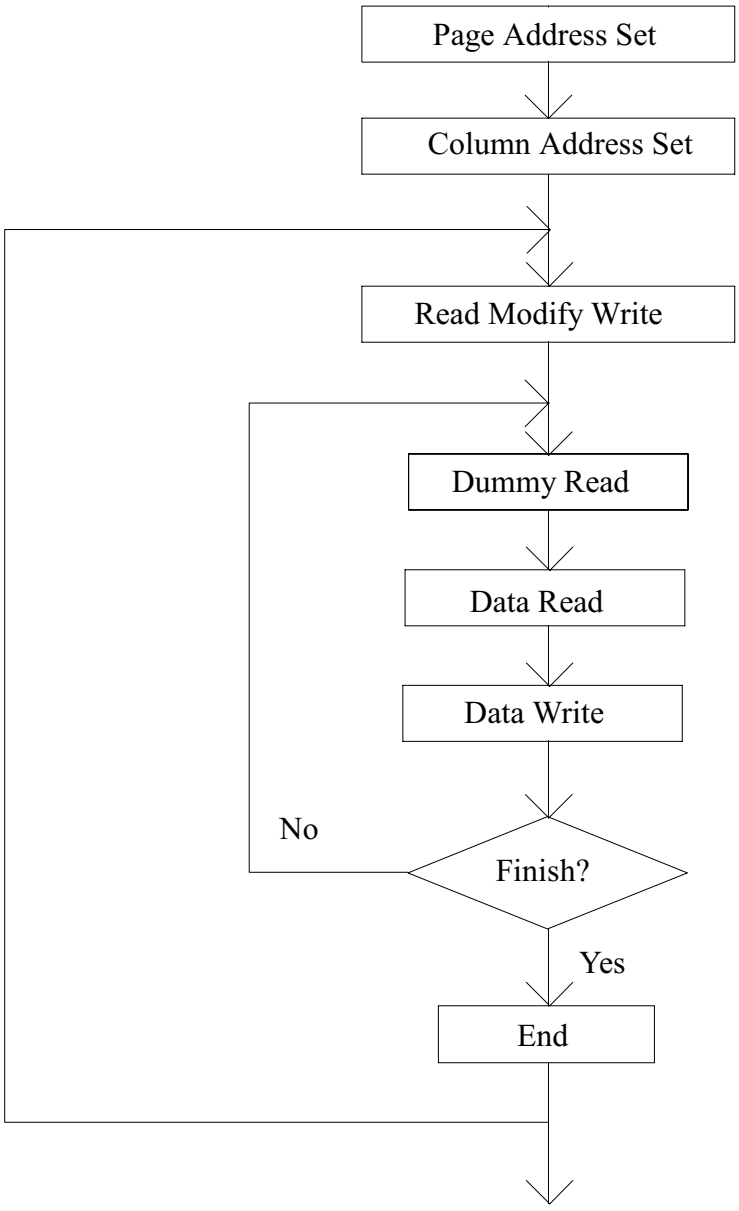
K. Read Modify Write

After this instruction is executed, the column address increase “1” automatically when Display Data Write Instruction execution, but the address is not changed when the Display Data Read Instruction execution.
This status continues during End instruction execution. When the End instruction is entered the column address back to the address where Read Modify Write instruction entering. By this function, the load of MPU for example cyclic data writing operation like as cursor blink etc., can be reduced.

	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	0	1	1	1	0	0	0	0	0

(**Note**) During the Read Modify Write mode, any instruction except Column Address Set can be executed.

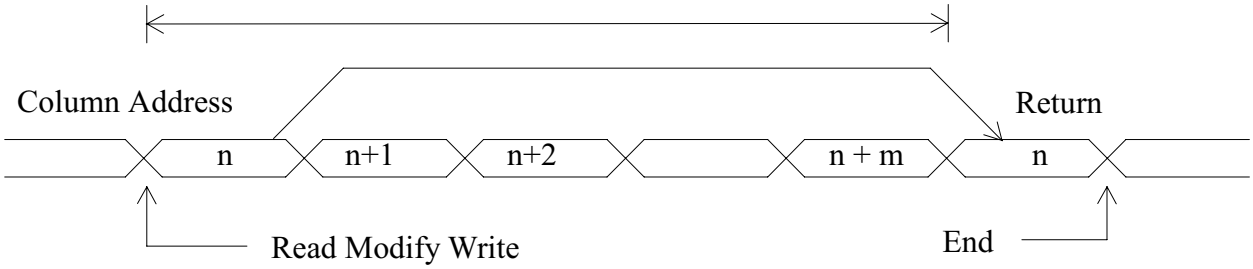
L. Sequence of cursor display



M. End

This instruction release the Read Modify Write mode and the column address back to the address where the Read Modify Write mode setting.

	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	0	1	1	1	0	1	1	1	0



N. Reset

This instruction executes the following initialization.

Initialization

1) Set the first line in the Display Start Line Register.
2) Set the page 3 in the Page Register.

In this time, there are no influence to the Display Data RAM.

	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Code	0	0	1	1	1	0	0	0	1	0

(**Note**) The initialization when the power terns on can no be executed by Reset instruction.

O. Power Save(Dual Command)

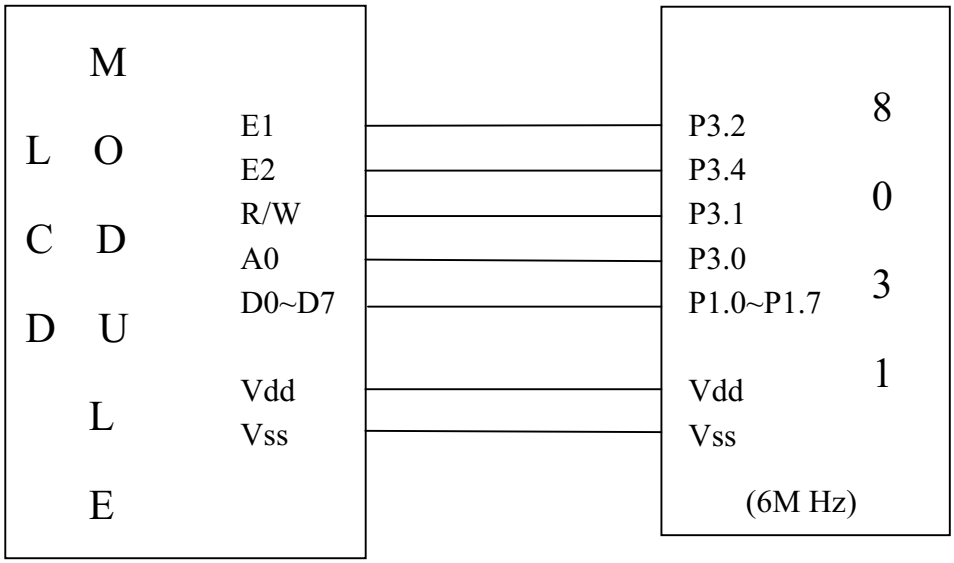
When both of Display Off and Static Drive On are executed, the internal put on the power save mode and the current consumption is reduced as same as stand by current. The internal status in this mode are as follows;

1) Stop the LCD driving. Segment and Common drivers output V_{dd} level.
2) Stop the oscillation or inhibit the external clock input.
3) Keeping the display data and operating mode.

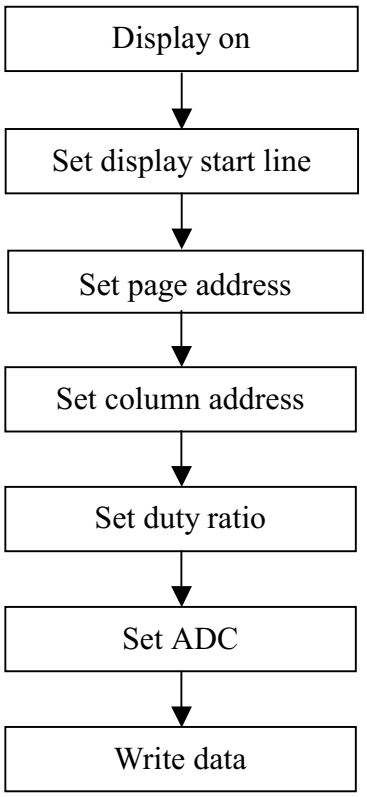
The power save mode is released by Display on or static drive off instruction.

● Application Example

Application Circuit



Application Flowchart



Program Example

```
;*********************************************
;       P3.0    P3.1    P3.2    P3.4
;       A0      R/W     E1      E2
;*********************************************
        A0      EQU     P3.0
        R/W     EQU     P3.1
        E1      EQU     P3.2
        E2      EQU     P3.4
;*********************************************
ORG     0000H
        LCALL   T2
        SETB    E1
        SETB    E2
        SETB    R/W
        SETB    P3.3
        CLR     A0
        MOV     A, #0AFH ;DISPLAY ON
        MOV     P1,     A
        LCALL   WR1
        MOV     A, #0C0H    ;START LINE
        MOV     P1,     A
        LCALL   WR1
        MOV     A, #0B8H    ;PAGE ADDRESS SET
        MOV     P1,     A
        LCALL   WR1
        MOV     A, #00H     ;COLUMN ADDRESS SET
        MOV     P1,     A
        LCALL   WR1
        MOV     A, #0A9H    ;SETUP DUTY
        MOV     P1,     A
        LCALL   WR1
        MOV     A, #0A0H    ;SETUP ADC
        MOV     P1,     A
        LCALL   WR1

        MOV     A, #0AFH ;DISPLAY ON
        MOV     P1,     A
        LCALL   WR2
```

```
        MOV   A, #0C0H   ;START LINE
        MOV   P1,     A
        LCALL    WR2
        MOV   A, #0B8H   ;PAGE ADDRESS SET
        MOV   P1,     A
        LCALL   WR2
        MOV   A, #00H   ;COLUMN ADDRESS SET
        MOV   P1,     A
        LCALL   WR2
        MOV   A, #0A9H   ;SETUP DUTY
        MOV   P1,     A
        LCALL   WR2
        MOV   A, #0A0H   ;SETUP ADC
        MOV   P1,     A
        LCALL   WR2
;*********************************************
MAIN:
        LCALL   AA3
        MOV   R1,#0B8H
        MOV   DPTR,#TAB1
        LCALL   LOOP122
        LCALL   AA4
        MOV   R1,#0B8H
        MOV   DPTR,#TAB12
        LCALL   LOOP121
       LCALL   T2

        SETB     R/W
        LCALL    AA3
        MOV      R1,     #0B8H   ;SHEN ZHEN JING HUA
        MOV      DPTR,   #TAB1A
        LCALL    LOOP122
        LCALL    AA4
        MOV      R1,     #0B8H   ;SHEN ZHEN JING HUA
        MOV      DPTR,   #TAB1B
        LCALL    LOOP121
        LCALL   T2
        AJMP    MAIN
;*********************************************
```

```
LOOP122:MOV   R6,#04H
LO122:  MOV     R2,    #3DH
        SETB    A0
JJ300:  CLR     A
        MOVC    A,     @A+DPTR
        MOV     P1,    A
        LCALL   WR1
        INC     DPTR
        DJNZ    R2,    JJ300
        CLR     A0
        MOV     A,#00H
        MOV     P1,A
        LCALL   WR1
        INC     R1
        MOV     P1,R1
        LCALL   WR1
        DJNZ   R6,LO122
        RET
;************************************************
LOOP121:MOV   R6,#04H
LO121:  MOV     R2,    #3DH
        SETB    A0
JJ30:   CLR     A
        MOVC    A,     @A+DPTR
        MOV     P1,    A
        LCALL   WR2
        INC     DPTR
        DJNZ    R2,    JJ30
        CLR     A0
        MOV     A,#00H
        MOV     P1,A
        LCALL   WR2
        INC     R1
        MOV     P1,R1
        LCALL   WR2
        DJNZ   R6,LO121
        RET
;************************************************
AA3:    CLR    A0
```

```
        MOV   A, #0C0H   ;START LINE
        MOV   P1,     A
        LCALL    WR1
        MOV   A, #0B8H   ;PAGE ADDRESS SET
        MOV   P1,     A
        LCALL    WR1
        MOV   A, #00H   ;COLUMN ADDRESS SET
        MOV   P1,     A
        LCALL    WR1
        RET
AA4:    CLR   A0
        MOV   A, #0C0H   ;START LINE
        MOV   P1,     A
        LCALL    WR2
        MOV   A, #0B8H   ;PAGE ADDRESS SET
        MOV   P1,     A
        LCALL    WR2
        MOV   A, #00H   ;COLUMN ADDRESS SET
        MOV   P1,     A
        LCALL    WR2
        RET
;****************************************
WR:     CLR   R/W
        NOP
        NOP
        SETB   E1
        SETB   E2
        LCALL   T1
        CLR   E1
        CLR   E2
        LCALL   T1
        SETB   E1
        SETB   E2
        SETB   R/W
        RET
;****************************************
WR1:    CLR   R/W
        SETB   E1
        LCALL   T1
```

```
        CLR   E1
        LCALL  T1
        SETB   E1
        SETB   R/W
        RET
;****************************************
WR2:    CLR  R/W
        SETB   E2
        LCALL  T4
        CLR   E2
        LCALL  T4
        SETB   E2
        SETB   R/W
        RET
;****************************************
T1:     MOV   R4,     #0BH
TTT1:   DJNZ   R4,    TTT1
        RET
T4:     MOV   R4,     #10H
TTTA:   DJNZ   R4,    TTTA
        RET
;****************************************
T2:     MOV   R7,#01H
T22:    MOV   R3, #0AFH
TT2:    MOV   R4,#0FFH
TTT2:   DJNZ   R4,    TTT2
        DJNZ   R3,    TT2
        DJNZ   R7,    T22
        RET
;****************************************
TT3:    MOV   R7,#01H
TT22:   MOV   R3,#0FH
TTT21:  MOV   R4,     #0FFH
TTTT2:  DJNZ   R4,    TTTT2
        DJNZ   R3,    TTT21
        DJNZ   R7,    TT22
        RET
;**********************IC1************************
TAB1:    DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
```

```
        DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
        DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
        DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
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        DB 0FFH,0FFH,0FFH,0FFH,0FFH
        DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
        DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
        DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
        DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
        DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
        DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
        DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
        DB 0FFH,0FFH,0FFH,0FFH,0FFH
        DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
        DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
        DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
        DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
        DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
        DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
        DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
        DB 0FFH,0FFH,0FFH,0FFH,0FFH
;**********************IC2************************
TAB12:  DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
        DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
        DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
        DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
        DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
        DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
        DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
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            DB 0FFH,0FFH,0FFH,0FFH,0FFH
            DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
            DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
            DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
            DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
            DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
            DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
            DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
            DB 0FFH,0FFH,0FFH,0FFH,0FFH
            DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
            DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
            DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
            DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
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            DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
            DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
            DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
            DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
            DB 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
            DB 0FFH,0FFH,0FFH,0FFH,0FFH
;****************************************************
;           DISPLAY    SHEN ZHENG JING HUA HAN ZI
;**********************IC1*************************
TAB1A:      DB 00H,00H,00H,00H,00H,00H,00H,70H
            DB 88H,88H,10H,00H,00H,0F8H,80H,80H
            DB 80H,0F8H,00H,00H,0F8H,88H,88H,88H
            DB 00H,00H,0F8H,10H,0E0H,80H,00H,0F8H
            DB 00H,00H,00H,08H,08H,0C8H,38H,08H
            DB 00H,00H,0F8H,80H,80H,80H,0F8H,00H
            DB 00H,0F8H,88H,88H,88H,00H,00H,0F8H
            DB 10H,0E0H,80H,00H,00H
            DB 00H,00H,00H,00H,00H,00H,00H,04H
            DB 08H,08H,07H,00H,00H,0FH,00H,00H
            DB 00H,0FH,00H,00H,0FH,08H,08H,08H
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        DB 00H,00H,0FH,00H,00H,03H,04H,0FH
        DB 00H,00H,00H,0CH,0BH,08H,08H,08H
        DB 00H,00H,0FH,00H,00H,00H,0FH,00H
        DB 00H,0FH,08H,08H,08H,00H,00H,0FH
        DB 00H,00H,03H,04H,00H

        DB 00H,00H,00H,00H,00H,00H,00H,00H
        DB 00H,00H,00H,00H,00H,00H,10H,10H
        DB 0F0H,10H,10H,00H,0F0H,50H,50H,10H
        DB 00H,0F0H,00H,00H,00H,40H,00H,00H
        DB 0E0H,10H,00H,0E0H,10H,10H,0E0H,00H
        DB 0E0H,10H,10H,0E0H,00H,0A0H,50H,50H
        DB 0A0H,00H,0E0H,50H,50H,0D0H,00H,10H
        DB 0E0H,00H,0E0H,10H,00H

        DB 00H,00H,00H,00H,00H,00H,00H,00H
        DB 00H,00H,00H,00H,00H,00H,00H,00H
        DB 01H,00H,00H,00H,01H,01H,01H,01H
        DB 00H,01H,01H,01H,00H,01H,00H,00H
        DB 00H,01H,00H,00H,01H,01H,00H,00H
        DB 00H,01H,01H,00H,00H,00H,01H,01H
        DB 00H,00H,00H,01H,01H,00H,00H,01H
        DB 00H,00H,00H,01H,00H

;**********************IC2************************
TAB1B:  DB 0F8H,00H,00H,00H,00H,00H,00H,00H,00H
        DB 00H,08H,08H,0F8H,08H,08H,00H,0F8H
        DB 00H,00H,0F8H,10H,0E0H,80H,00H,0F8H
        DB 00H,00H,0E0H,10H,08H,08H,08H,08H
        DB 00H,00H,00H,0F8H,80H,80H,80H,0F8H
        DB 00H,00H,0F8H,00H,00H,00H,00H,0F8H
        DB 00H,00H,0C0H,0A0H,90H,88H,90H,0A0H
        DB 0C0H,00H,00H,00H

        DB 0FH,00H,00H,00H,00H,00H,00H,00H,00H
        DB 06H,08H,08H,07H,00H,00H,00H,0FH
        DB 00H,00H,0FH,00H,00H,03H,04H,0FH
        DB 00H,00H,03H,04H,08H,08H,09H,07H
        DB 01H,00H,00H,0FH,00H,00H,00H,0FH
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    DB 00H,00H,03H,04H,08H,08H,04H,03H
    DB 00H,00H,0FH,00H,00H,00H,00H,00H
    DB 0FH,00H,00H,00H

    DB 10H,0E0H,00H,10H,90H,50H,30H,00H,70H
    DB 50H,0D0H,00H,70H,50H,0D0H,00H,40H
    DB 40H,40H,40H,00H,90H,50H,20H,00H
    DB 0C0H,0A0H,0F0H,80H,00H,90H,50H,20H
    DB 00H,0E0H,10H,0E0H,00H,10H,50H,0A0H
    DB 00H,20H,50H,50H,0E0H,00H,10H,50H
    DB 0A0H,00H,00H,00H,00H,00H,00H,00H
    DB 00H,00H,00H,00H

    DB 01H,00H,00H,01H,00H,00H,00H,00H,01H
    DB 01H,01H,00H,01H,01H,01H,00H,00H
    DB 00H,00H,00H,00H,01H,01H,01H,00H
    DB 00H,00H,01H,00H,00H,01H,01H,01H
    DB 00H,00H,01H,00H,00H,01H,01H,00H
    DB 00H,00H,01H,01H,00H,00H,01H,01H
    DB 00H,00H,00H,00H,00H,00H,00H,00H
    DB 00H,00H,00H,00H
END
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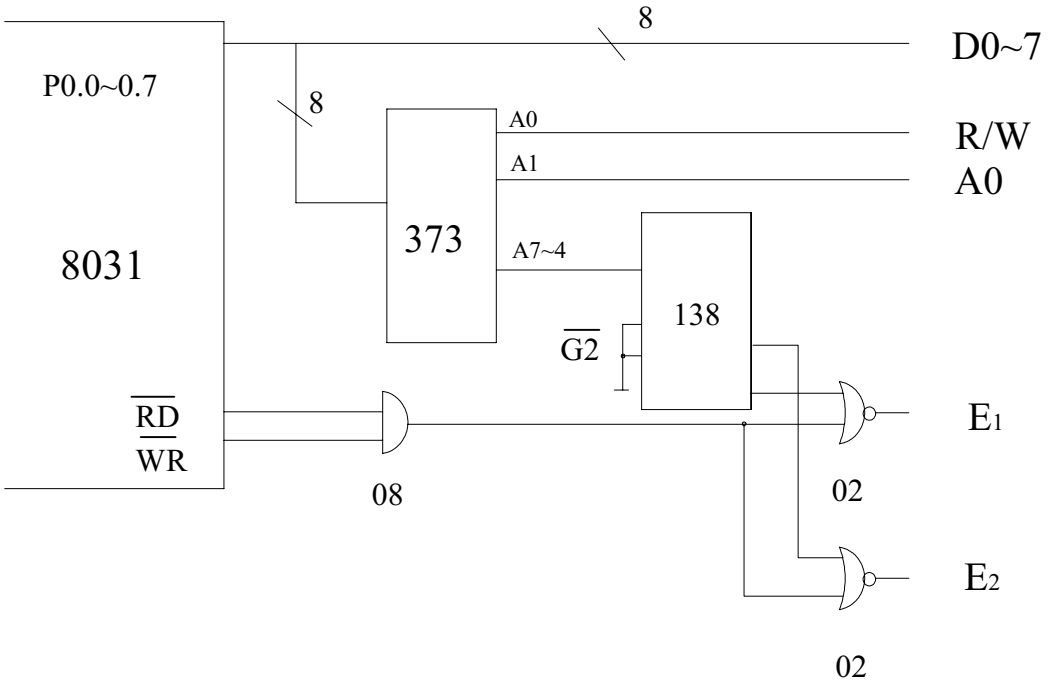
● Application Circuit 1



● Application Circuit 2