Princeton Technology Corp.
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# DESCRIPTIONS

PT6607 is a 64-channel common driver for dot matrix liquid crystal graphic display system. It utilizes CMOS technology and provides 64 shift registers and 64 output drivers. PT6607 generates the timing signal which controls the PT6608 segment driver. Pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantages.

# FEATURES

- CMOS technology
- 64 channel outputs
- Provides 64 bits shift register in the internal LCD driver circuit
- Internal timing generator circuit for dynamic display
- Selectable master/slave mode
- Power supply: + 5V + 10 %
- LCD driving voltage: 8V to 17V (VDD-VEE)
- LCD duty: 1/48, 1/64, 1/96, 1/128
- Available in C.O.B. or 100-pin, QFP package
- Interface:
    - common driver -- PT6607
    - segment driver -- PT6608

# APPLICATIONS

- Peripheral devices

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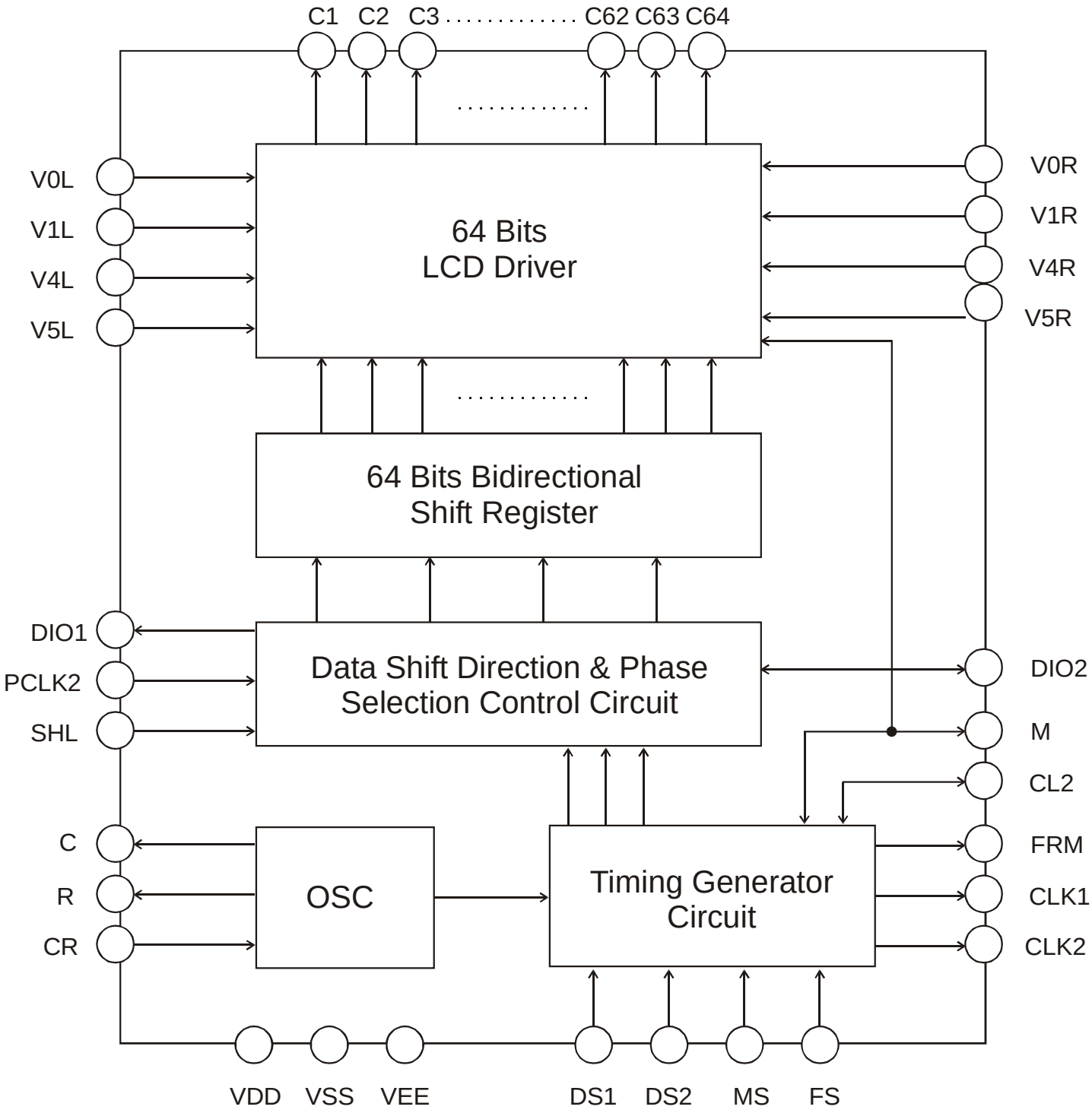
# BLOCK DIAGRAM



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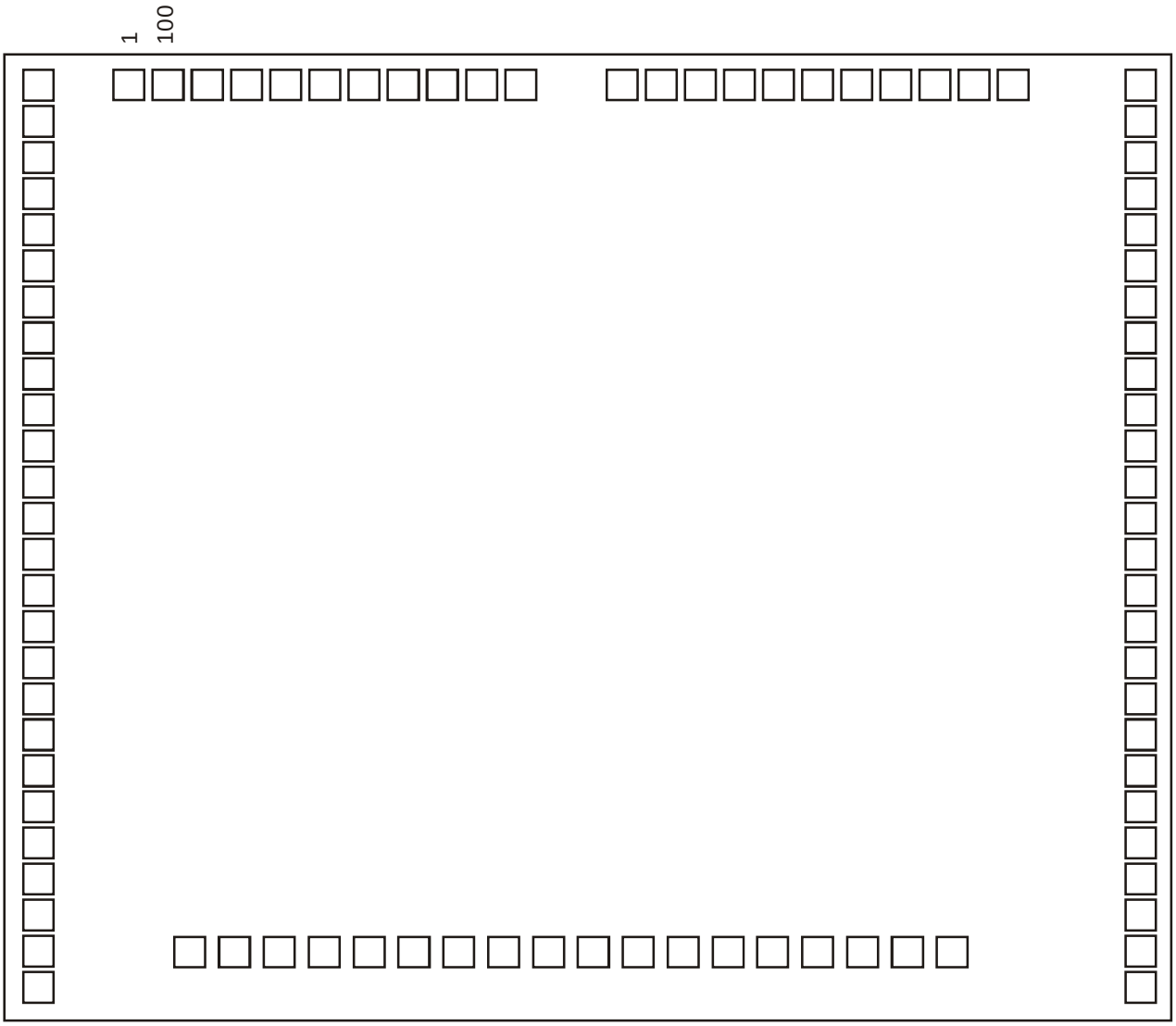
# PIN CONFIGURATION



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# PIN DESCRIPTION

| Pin Name | I/O | Description | Pin No. |
|---|---|---|---|
| C22 ~ C1 | O | Common Signal Output Pins | 1 ~ 22 |
| VEE | - | Power Supply for LCD Driver Circuit | 23,58 |
| V1L | - | Bias Supply Voltage Pin | 24 |
| V4L | - | Bias Supply Voltage Pin | 25 |
| V5L | - | Bias Supply Voltage Pin | 26 |
| V0L | - | Bias Supply Voltage Pin | 27 |
| VDD | - | Power Supply for Internal Logic Circuit | 28 |
| DIO1,DIO2 | I/O | Internal Shift Register Data Input/Output Pin | 29,50 |
| FS | I | Frequency Select Pin | 30 |
| DS1, DS2 | I | Display Duty Select Pin | 31, 32 |
| C | - | Oscillator Pin | 33 |
| NC | - | No Connection | 34,38,41,45,48,51,53 |
| R | - | Oscillator Pin | 35 |
| CR | - | Oscillator Pin | 37 |
| SHL | I | Data Shift Direction Select Pin | 39 |
| VSS | - | GND (0V) | 40 |
| MS | I | Master/Slave Select Pin | 42 |
| CLK1, CLK2 | O | Operating Clock Output Pin | 44,43 |
| FRM | O | Synchronous Frame Signal Output Pin | 46 |
| | | Under the Slave Mode, this pin is “Open”. | |
| M | I/O | Alternating Signal Pin | 47 |
| PCLK2 | I | Shift Clock Select Pin | 49 |
| CL2 | I/O | Data Shift Clock Input/Output Pin | 52 |
| V0R | - | Bias Supply Voltage Pin | 54 |
| V5R | - | Bias Supply Voltage Pin | 55 |
| V4R | - | Bias Supply Voltage Pin | 56 |
| V1R | - | Bias Supply Voltage Pin | 57 |
| C64~C23 | O | Common Signal Output Pins | 59~100 |

# FUNCTIONAL DESCRIPTION

## *MODE SELECTION*

PT6607 may be selected to act as a master or a slave. This master/slave selection is controlled by MS Pin.

### MASTER MODE

To select the Master Mode, MS must be set to “1”. Under this mode, Input/Output Pins --DIO1, DIO2, CL2 and M are acting only as Output Pins.
Please refer to table below.

### SLAVE MODE

To select the Slave Mode, MS must be set to “0”. Under this mode, Input/Output Pins -- CL2 and M acts only as an Input Pin. DIO1 and DIO2 state will depend on the SHL setting. Please refer to the table below.

| | MS Pin | SHL Pin | DIO1 Pin State | DIO2 Pin State |
|---|---|---|---|---|
| Master Mode | “1” | “1” | Output | Output |
| | | “0” | Output | Output |
| Slave Mode | MS Pin | SHL Pin | DIO1 Pin State | DIO2 Pin State |
| | “0” | “1” | Input | Output |
| | | “0” | Output | Input |

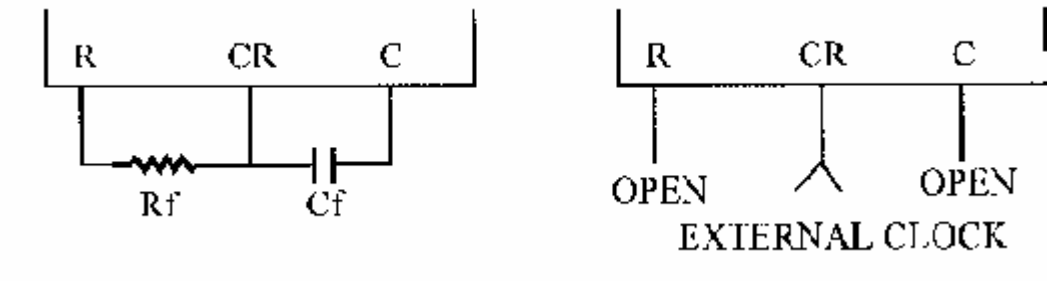
## *COMMON SIGNAL OUTPUT (LCD DRIVE)*

| Data | M | OUT |
|---|---|---|
| L | L | V1 |
| L | H | V4 |
| H | L | V5 |
| H | H | V0 |

# OSCILLATION CIRCUIT

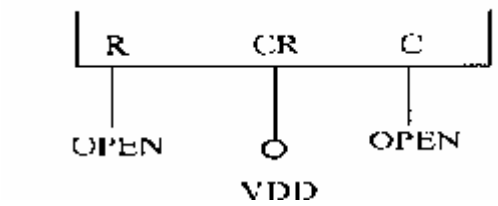
## MASTER MODE

In the Master Mode, the Oscillation Circuit may be constructed as follows:




## SLAVE MODE

In the Slave Mode, the Oscillation Circuit may be constructed as follows.




# OSCILLATION FREQUENCY SELECTION

Pin No. 30 -- FS Pin is the Oscillation Frequency Select Pin.

## MASTER MODE

When FRM Frequency is 70 Hz, the following conditions applies.

| Oscillation Frequency | FS Pin |
|---|---|
| fosc =430 kHz | 1 (connected to VDD) |
| fosc = 215 kHz | 0 (connected to VSS) |

## SLAVE MODE

Under the Slave Mode, FS Pin is connected to VDD.

# DISPLAY DUTY SELECTION

Various Display Duties may be selected depending on the states of inputs pins, DS1 and DS2.

## MASTER MODE

The table below shows the various display duties that may be selected and the corresponding DS1 and DS2 settings.

| DS1 | DS2 | Display Duty |
|---|---|---|
| L | L | 1/48 |
| L | H | 1/64 |
| H | L | 1/96 |
| H | H | 1/128 |

## SLAVE MODE

DS1 and DS2 Pins are connected to VDD when the Slave Mode is enabled.

# SHIFT CLOCK OR PHASE SELECTION

PCLK2 may be set to shift data on the rising or falling edge of the CL2. The table below shows how the phase selection setting.

| PCLK2 Setting | Phase Selection |
|---|---|
| H | Data Shift at the Rising Edge of the CL2 |
| L | Data Shift at the Falling Edge of the CL2 |

# DATA SHIFT DIRECTION SELECTION

The Data Shift Direction may be selected according to the table below:

| | MS | SHL | DIO1 State | DIO2 State | Direction of Data |
|---|---|---|---|---|---|
| Master Mode | "1" | "1" | Output | Output | C1-->C64 |
| | | "0" | Output | Output | C64-->C1 |
| Slave Mode | MS | SHL | DIO1 State | DIO2 State | Direction of Data |
| | "0" | "1" | Input | Output | DIO1-->C1-->C64-->DIO2 |
| | | "0" | Output | Input | DIO2-->C64-->C1-->DIO1 |

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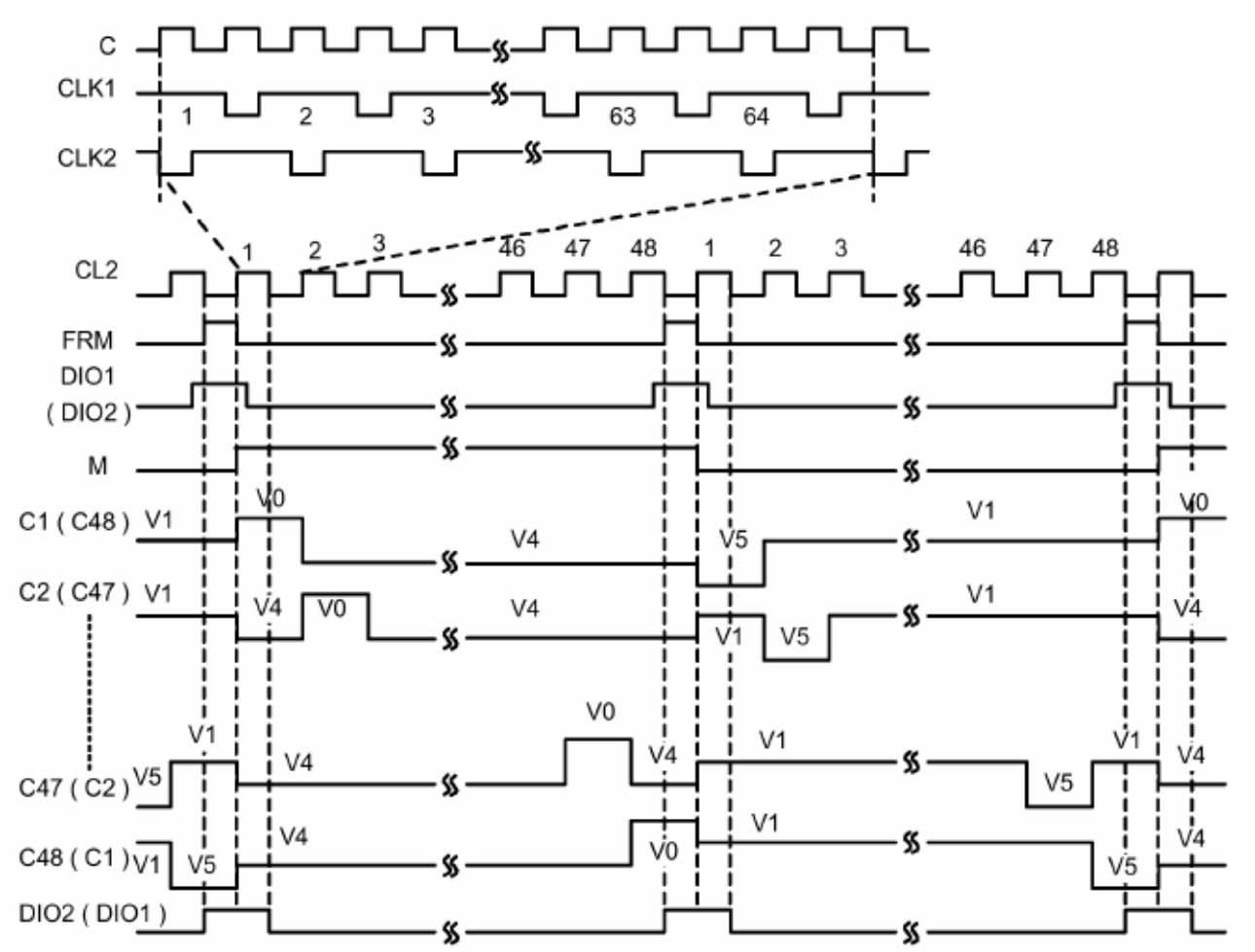
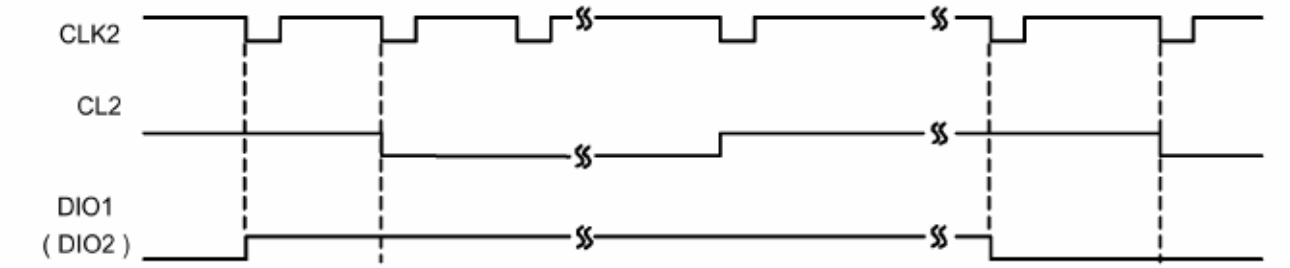
# TIMING DIAGRAM

## *MASTER MODE: 1/48 DUTY TIMING*

Conditions: DS1="L", DS2="L", SHL="H"("L"), PCLK2="H"




- relation of CL2 & DIO1 ( DIO2 )



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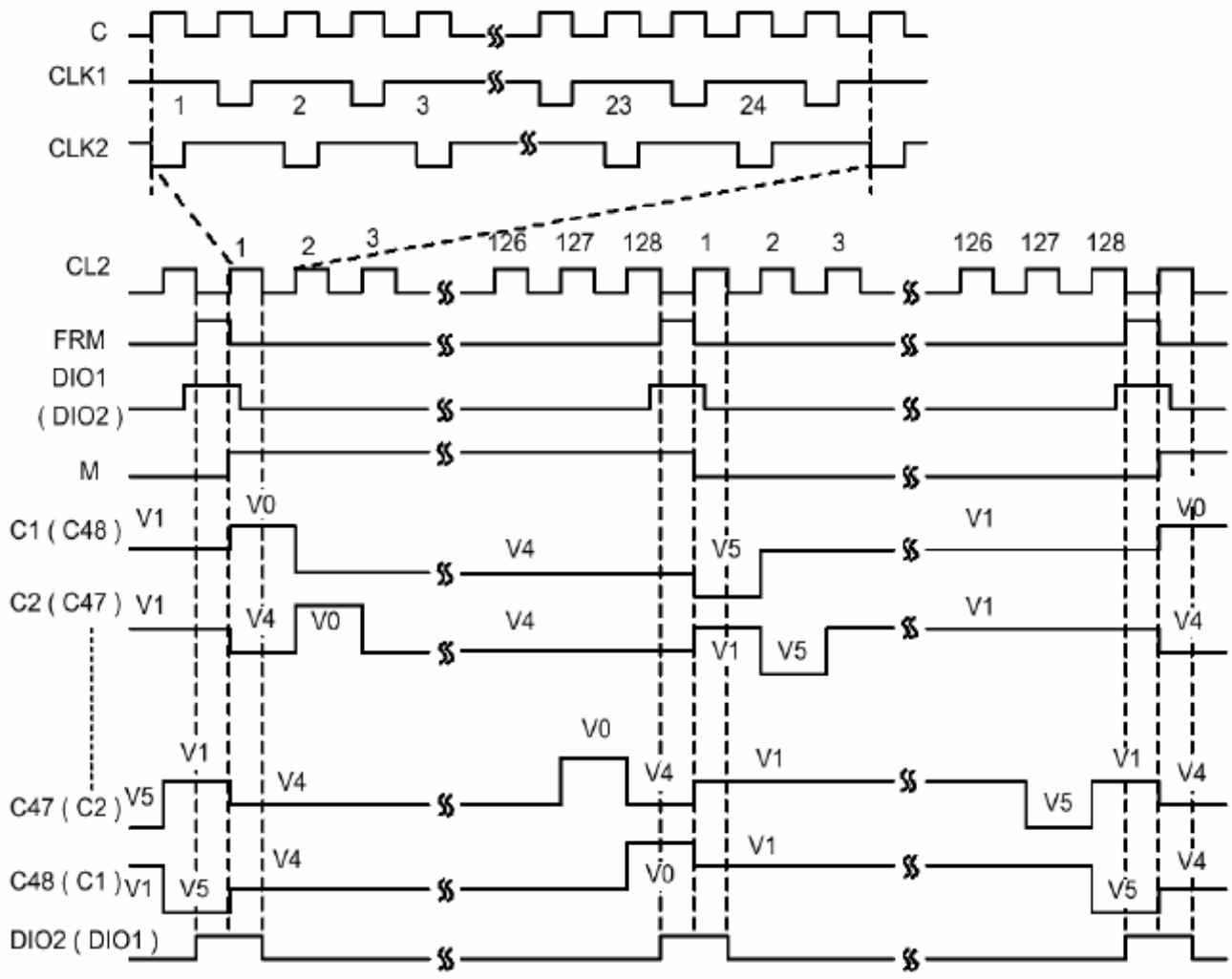
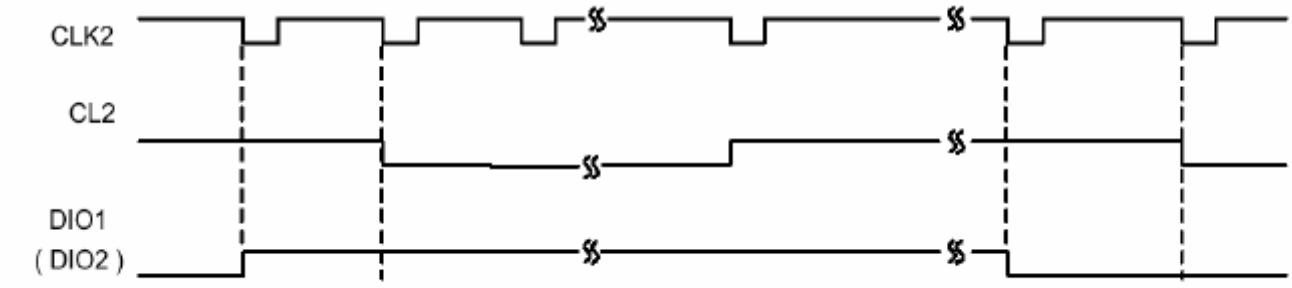
## *MASTER MODE: 1/128 DUTY TIMING*

Conditions: DS1="H", DS2="H", SHL="H"("L"), PCLK2="H"




- relation of CL2 & DIO1 ( DIO2 )



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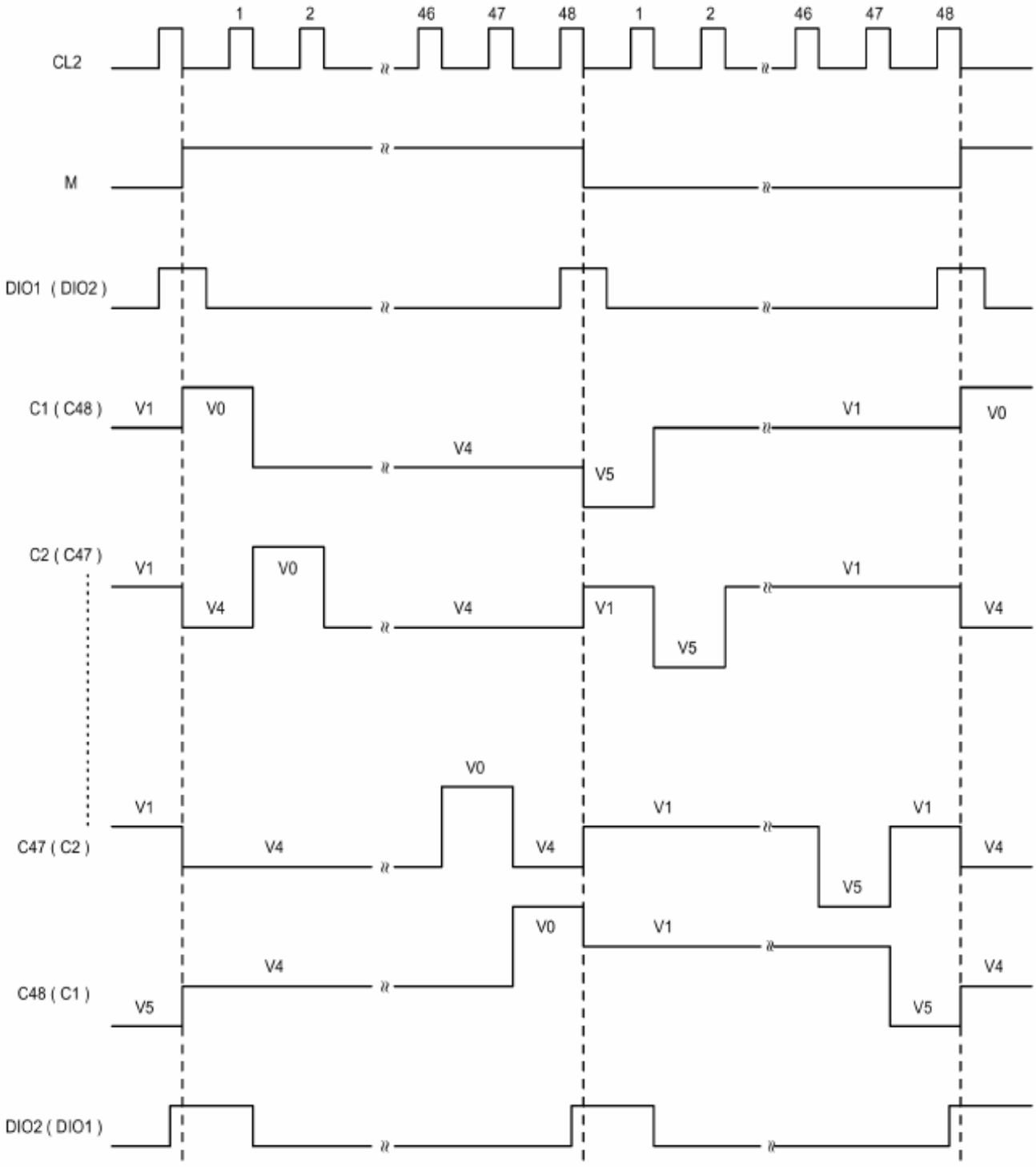
## *SLAVE MODE: 1/48 DUTY TIMING*

Conditions: PCLK2="l", SHL="H"("L")



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# ABSOLUTE MAXIMUM RATING

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Operating Voltage | VDD | -0.3 to +7.0 **(see Note 1)** | V |
| Supply Voltage | VEE | VDD -19.0 to VDD +0.3 **(see Note 4)** | V |
| Driver Supply Voltage | VB | -0.3 to VDD +0.3 **(see Notes 1 & 2)** | V |
| | VLCD | -0.3 to VDD +0.3 **(see Notes 3 & 4)** | V |
| Operating Temperature | TOPR | -30 to +85 | °C |
| Storage Temperature | TSTG | -55 to +125 | °C |

Notes:

1. Based on VSS=0V
2. Applies to Input terminals and I/OTerminals at High Impedance (Except V0L, V0R, V4L,V4R, V5L, V5R)
3. Applies to V0L, V0R, V4L,V4R, V5L, and V5R.
4. Voltage Level: VDD > V0L=V0R > V1L=V1R > V4L=V4R > V5L=V5R > VEE

# ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, VDD= +5V + 10 %, VSS=0V, |VDD-VEE | =8 to 17V, Ta=-30 to +85 oC)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| High Level Input Voltage **(see Note 1)** | VIH | - | 0.7VDD | - | VDD | V |
| Low Level Input Voltage **(see Note 1)** | VIL | - | VSS | - | 0.3VDD | V |
| High Level Output Voltage **(see Note 2)** | VOH | IOH = -0.4mA | VDD – 0.4 | - | - | V |
| Low Level Output Voltage **(see Note 2)** | VOL | IOL = 0.4mA | - | - | 0.4 | V |
| Input Leakage Current **(see Note 1)** | ILKG | VIN = VDD to VSS | -1.0 | - | 1.0 | μA |
| OSC Frequency | fosc | Rf = 47KOhms ± 2%<br>Cf = 20 pf ± 5% | 315 | 450 | 585 | kHz |
| On Resistance<br>Vdiv - Ci | Ron | VDD – VEE = 17V<br>Load Current ± 150μA | - | - | 1.5 | kOhms |
| Operating Current **(see Note 3)** | IDD1 | Master Mode<br>1/128 Duty | - | - | 1.0 | mA |
| | IDD2 | Slave Mode<br>1/128 Duty | - | - | 200 | μA |
| Supply Current **(see Note 4)** | IEE | Master Mode<br>1/128 Duty | - | - | 100 | μA |
| Operating Frequency | fop1 | Master Mode External Clock | 50 | - | 600 | kHz |
| | fop2 | Slave Mode | 0.5 | | 1500 | kHz |

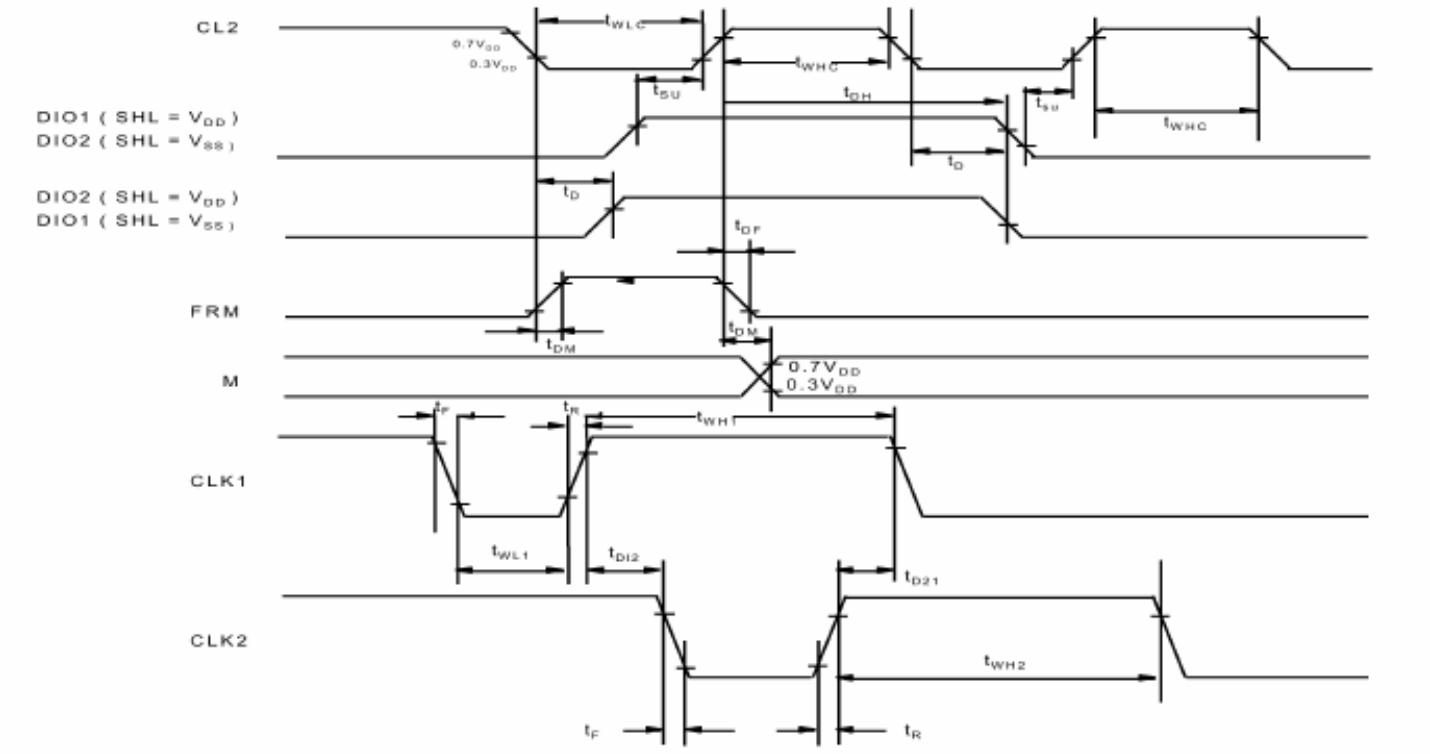
Notes:

1. Applies to Input Terminals: FS, DS1, DS2, CR, SHL, MS & PCLK2. Applies to I/O Terminals: DIO1, DIO2, M and CL2 in the Input State.
2. Applies to Output Terminals: CLK1, CLK2 and FRM. Applies to I/O Terminals: DIO1, DIO2, M and CL2 in the Output State.
3. Master Mode: This value is specified at about the current flowing through VSS. Internal Oscillation Circuit: Rf=47 k Ohms and Cf=20pF. Slave Mode: This value is specified at about the current flowing through VSS. Each Terminal (DS1, DS2, FS, SHL, PCLK2 and CR) is connected to VDD. MS is connected to VSS, CL2, M, DIO1 is external clock.
4. This value is specified at about the current flowing through VEE. Do not connect to VLCD (V1 to V5)

# AC CHARACTERISTICS: MASTER MODE

(Unless otherwise specified, VDD=5V + 10%, Ta=30oC to +85oC, MS=VDD, PCLK2=VDD, Cf=20pF, Rf=47KOhms)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Data Setup Time | tSU | 20 | - | - | uS |
| Data Hold Time | tDH | 40 | - | - | uS |
| Data Delay Time | tD | 5 | - | - | uS |
| FRM Delay Time | tDF | -2 | - | +2 | uS |
| M Delay Time | tDM | -2 | - | +2 | uS |
| CL2 Low Level Width | tWLC | 35 | - | - | uS |
| CL2 High Level Width | tWHC | 35 | - | - | uS |
| CLK1 Low Level Width | tWL1 | 700 | - | - | nS |
| CLK2 Low Level Width | tWL2 | 700 | - | - | nS |
| CLK1 High Level Width | tWH1 | 2100 | - | - | nS |
| CLK2 High Level Width | tWH2 | 2100 | - | - | nS |
| CLK1-CLK2 Phase Difference | tD12 | 700 | - | - | nS |
| CLK2-CLK1 Phase Difference | tD21 | 700 | - | - | nS |
| CLK1, CLK2 Rise / Fall Time | tR/tF | - | - | 150 | nS |



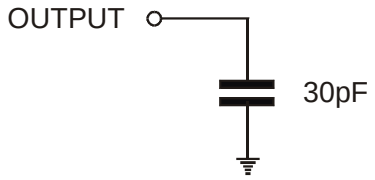
# AC CHARACTERISTICS: SLAVE MODE

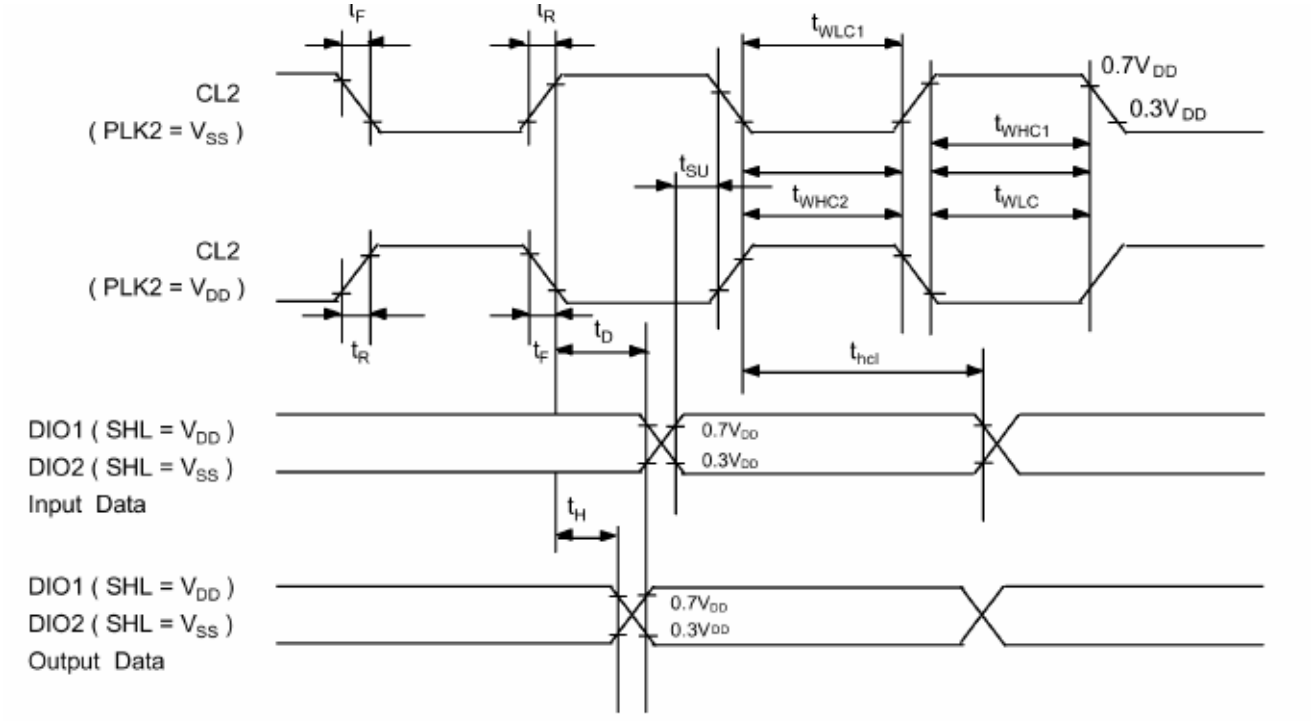
(Unless otherwise specified, VDD=5V + 10%, Ta=30oC to +85oC, MS=VSS)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| CL2 Low Level Width **(see Note 1)** | tWLC1 | 450 | - | - | nS |
| CL2 High Level Width **(see Note 1)** | tWHC1 | 150 | - | - | nS |
| CL2 Low Level Width **(see Note 2)** | tWLC2 | 150 | - | - | nS |
| CL2 High Level Width **(see Note 2)** | tWHL) | 450 | - | - | nS |
| Data Setup Time | tSU | 100 | - | - | nS |
| Data Hold Time | tDH | 100 | - | - | nS |
| Data Delay Time **(see Note 3)** | tD | - | - | 200 | nS |
| Output Data Hold Time | tH | 10 | - | - | nS |
| CL2 Rise / fall Time | tR/tF | - | - | 30 | nS |

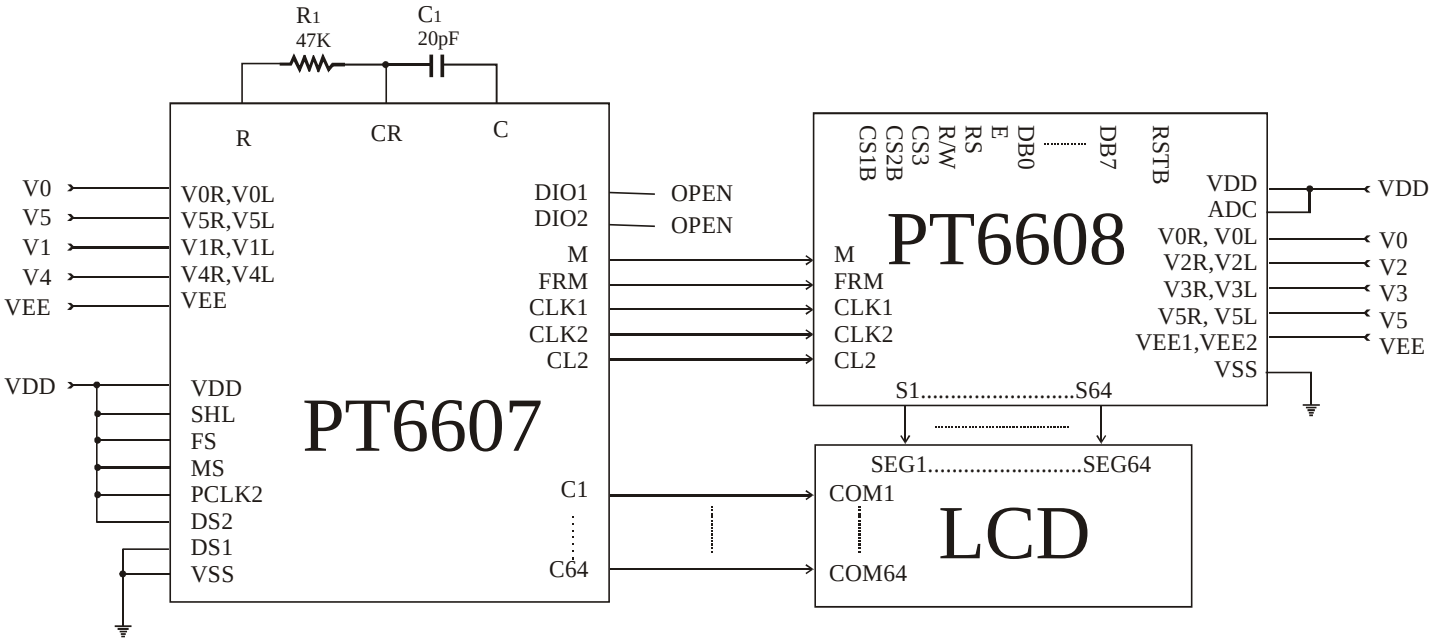
Notes:

1. PCLK2=VSS
2. PCLK2=VDD
3. Connect the load CL=30pF.

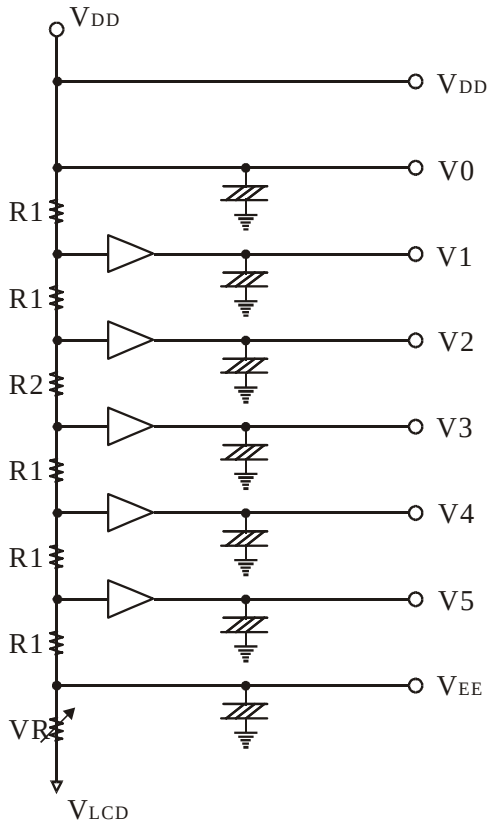


# APPLICATION CIRCUIT




## *POWER DRIVER CIRCUIT*




| Duty | Bias | Rdiv |
|---|---|---|
| 1/48 | 1/8 | R2=4R1 |
| 1/64 | 1/9 | R2=5R1 |
| 1/96 | 1/11 | R2=7R1 |
| 1/128 | 1/12 | R2=8R1 |

Notes:

1. When the duty factor is 1/48, the value of R1 and R2 must satisfy the following:
   R1/(4R1+R2)=1/8
   R1=3 k
   R2=12 k

2. Bias means division of voltage between VDD and VEE.
   Ex. 1/8 Bias means divide the voltage VDD and VEE to be 8 equalizers.

3. V1, V2, V3, V4, V5 and VEE voltage levels can be adjusted by the VR.

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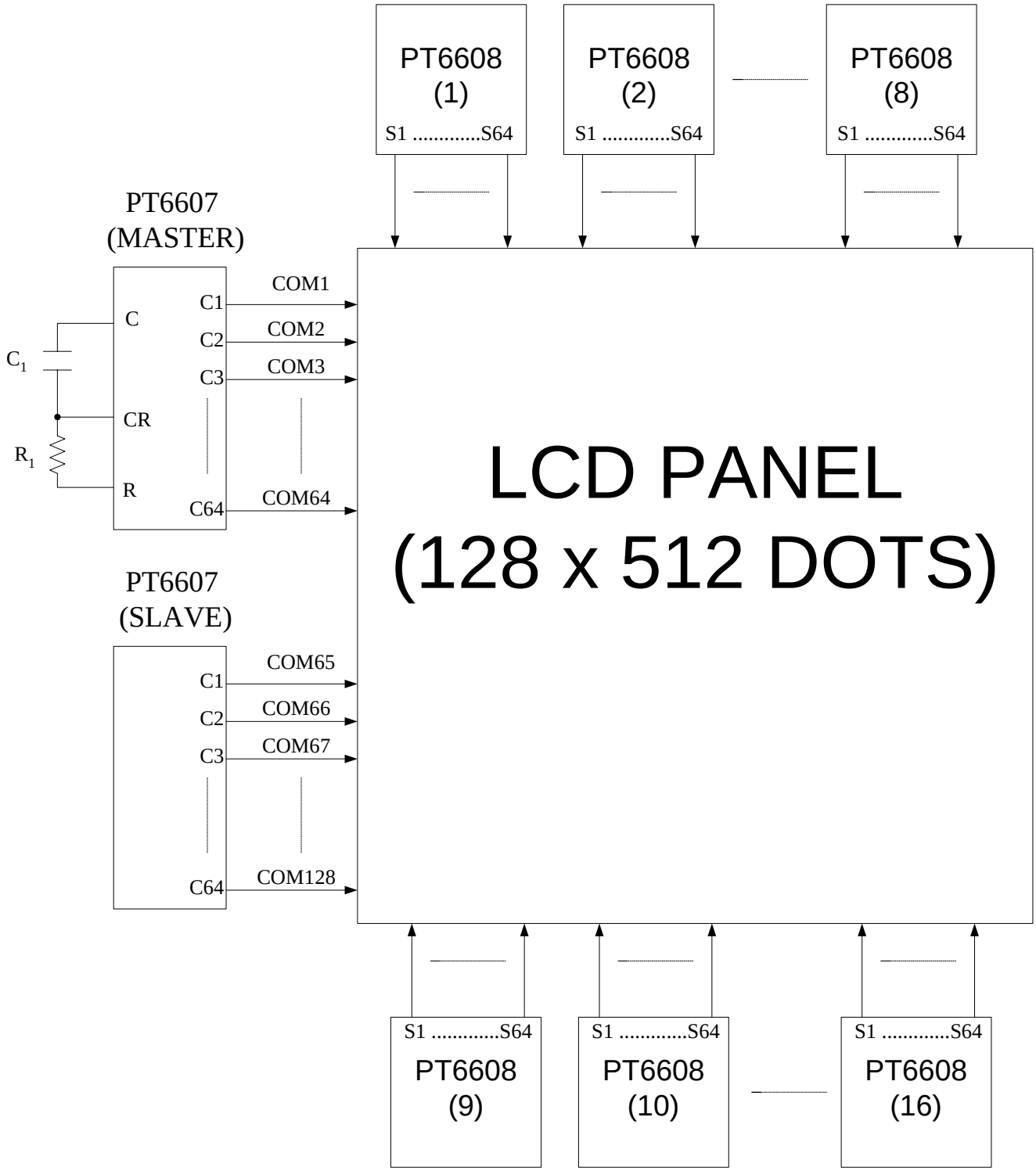
## *LCD PANEL INTERFACE APPLICATION CIRCUIT*



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# ORDER INFORMATION

| Valid Part Number | Package Type |
|---|---|
| PT6607 | 100 Pins, QFP Package |
| PT6607-H | C.O.B |

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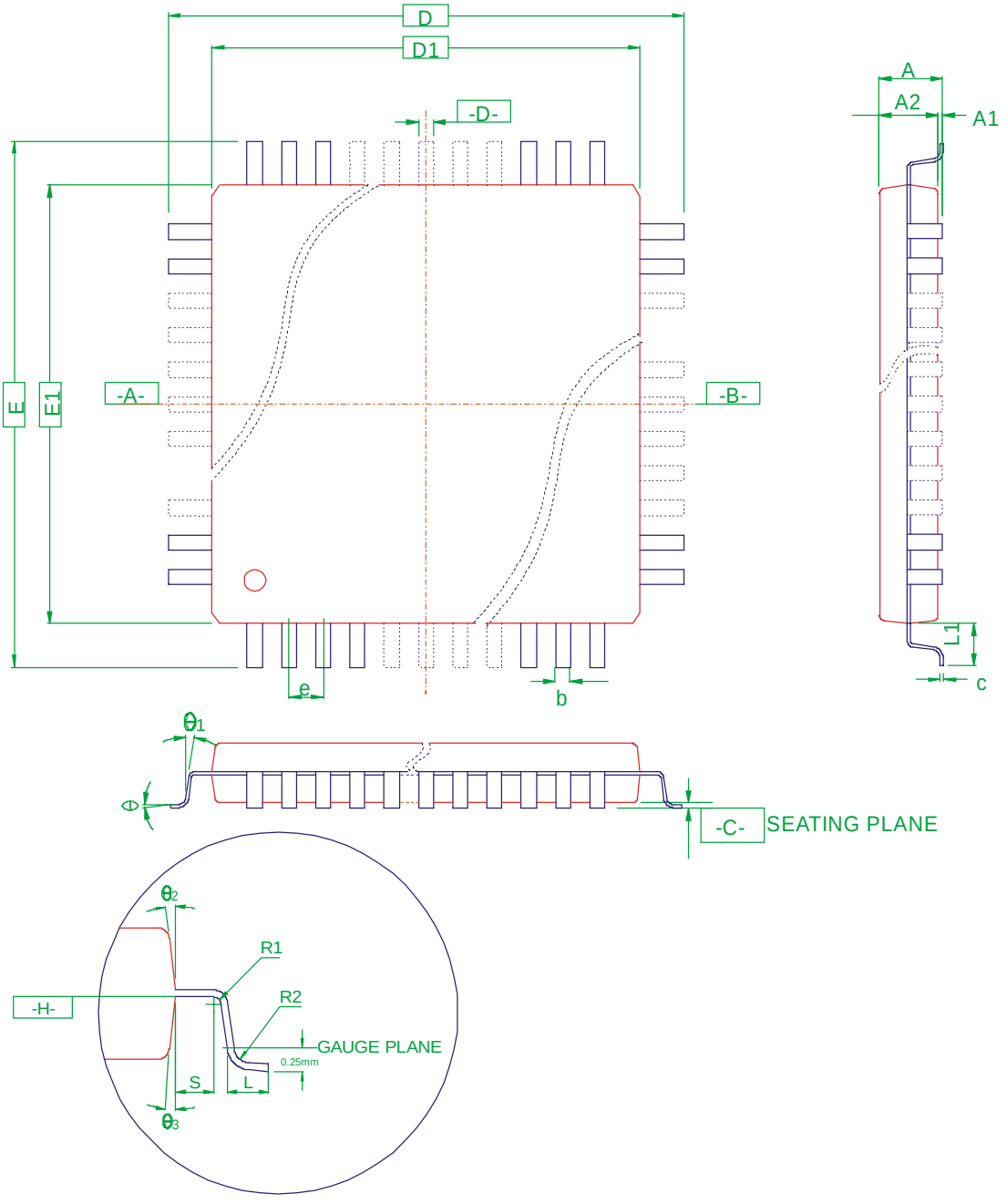
# PACKAGE INFORMATION

## *100 PINS, QFP PACKAGE (BODY SIZE: 20MM X 14MM, PITCH: 0.65MM)*



| Symbol | Min. | Nom. | Max |
|---|---|---|---|
| c | 0.11 | - | 0.23 |
| L | 0.73 | 0.88 | 1.03 |
| L1 | - | 1.60 | - |
| A | - | - | 3.40 |
| A1 | 0.25 | - | 0.50 |
| A2 | 2.50 | 2.70 | 2.90 |
| b | 0.22 | - | 0.40 |
| R1 | 0.13 | - | - |
| R2 | 0.13 | - | 0.30 |
| q | 0o | - | 7o |
| q1 | 0o | - | - |
| q2 | 5o | - | 16o |
| q3 | 5o | - | 16o |
| S | 0.20 | - | - |
| D | 23.20 BASIC | | |
| D1 | 20.00 BASIC | | |
| E | 17.20 BASIC | | |
| E1 | 14.00 BASIC | | |
| e | 0.65 BASIC | | |

Notes:

1. All dimensioning and tolerancing conform to ASME Y14.5M-1994
2. Dimensions D1 and E1 do not include mold protrusion, allowable protrusion is 0.25 mm per side, dimensions D1 and E1 do include mold mismatch and are determined at datum plane H".
3. Details of Pin 1 identifier are optional but must be located within the zone indicated.
4. Regardless of the relative size of the upper and lower body sections, dimensions D1 and E1 are determined at the largest feature of the body exclusive of mold flash and gate burrs but including any mismatch between the upper and lower sections of the molded body.
5. All dimensions are in millimeters.
6. Dimension b do not include dambar protrusion. The dambar protrusion(s) shall not cause the lead width to exceed B maximum by more than 0.08 mm. Dambar cannot be located on the lower radius or the lead foot.
7. A1 is defined as the distance from the seating plane to the lowest point of the package body.
8. Refer to JEDEC MS-022 Variation GC-1.

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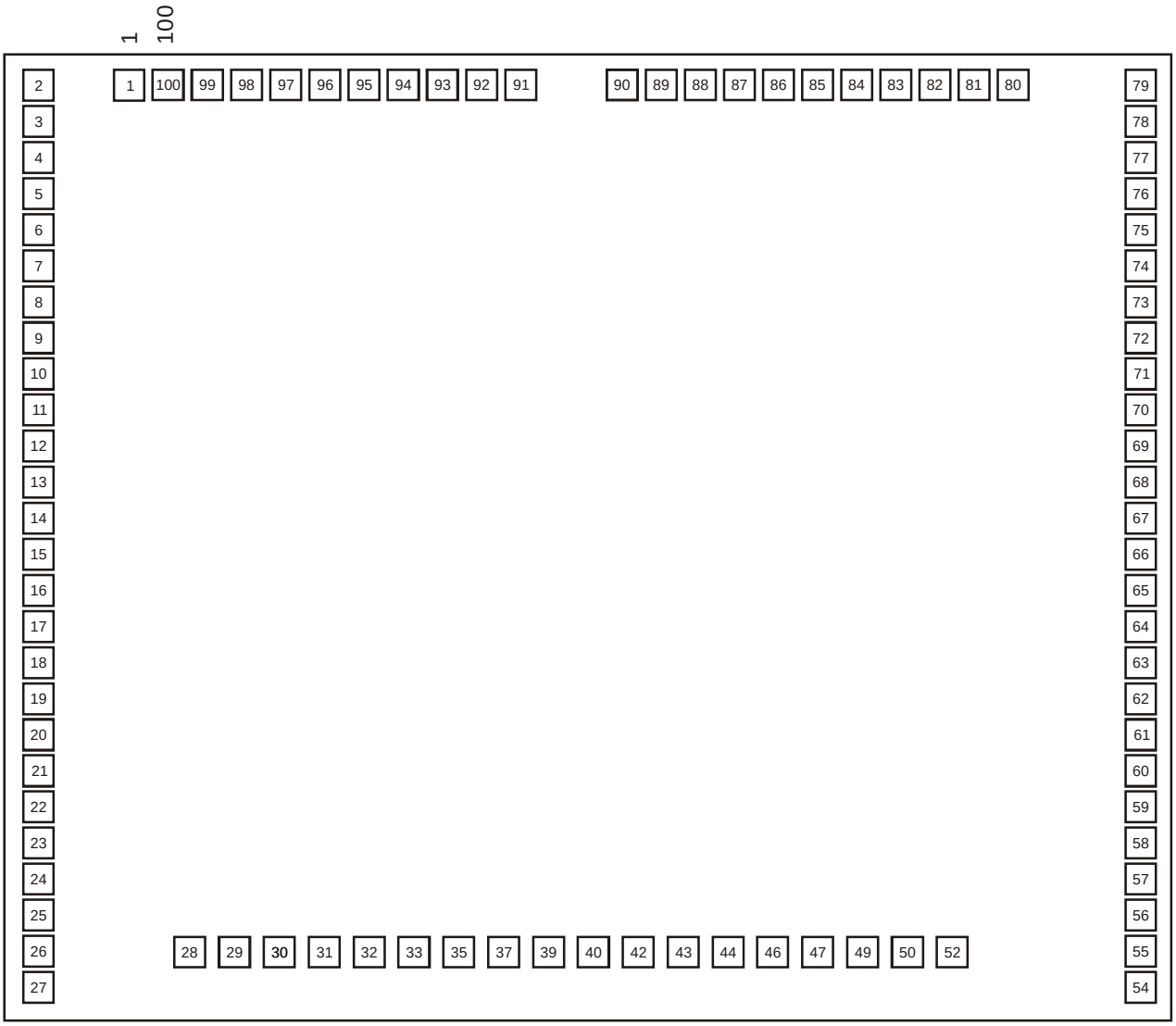
# PAD CONFIGURATION




Chip Size: 3067 x 3009.5 μm
Pad Size: 90 x 90 μm
Pitch: 110 μm

Note: * = The dice substrate is an n-substrate; therefore, it is recommended that it be connected to VDD. If it is connected to VSS, then there is a great possibility that the chip will be damaged.

# PAD LOCATION

| PAD Number | Name | Location |
|---|---|---|
| 1 | O22 | [338.900, 2935.600] |
| 2 | O21 | [73.900, 2918.400] |
| 3 | O20 | [73.900, 2808.400] |
| 4 | O19 | [73.900, 2698.400] |
| 5 | O18 | [73.900, 2588.400] |
| 6 | O17 | [73.900, 2478.400] |
| 7 | O16 | [73.900, 2368.400] |
| 8 | O15 | [73.900, 2258.400] |
| 9 | O14 | [73.900, 2148.400] |
| 10 | O13 | [73.900, 2038.400] |
| 11 | O12 | [73.900, 1928.400] |
| 12 | O11 | [73.900, 1818.400] |
| 13 | O10 | [73.900, 1708.400] |
| 14 | O9 | [73.900, 1598.400] |
| 15 | O8 | [73.900, 1488.400] |
| 16 | O7 | [73.900, 1378.400] |
| 17 | O6 | [73.900, 1268.400] |
| 18 | O5 | [73.900, 1158.400] |
| 19 | O4 | [73.900, 1048.400] |
| 20 | O3 | [73.900, 938.400] |
| 21 | O2 | [73.900, 828.400] |
| 22 | O1 | [73.900, 718.400] |
| 23 | VEE | [73.900, 608.400] |
| 24 | V1 | [74.400, 470.200] |
| 25 | V4 | [74.400, 346.200] |
| 26 | V5 | [74.400, 222.200] |
| 27 | V0 | [74.400, 98.200] |
| 28 | VCC | [554.100, 165.400] |
| 29 | DIO1 | [679.900, 165.400] |
| 30 | FS | [789.900, 165.400] |
| 31 | DS1 | [899.900, 165.400] |
| 32 | DS2 | [1009.900, 165.400] |
| 33 | C | [1119.900, 165.350] |
| 34 | NC | |
| 35 | R | [1229.900, 165.400] |
| 36 | NC | |
| 37 | CR | [1339.900, 165.400] |
| 38 | NC | |
| 39 | SHL | [1449.900, 165.400] |
| 40 | GND | [1563.800, 165.400] |

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| PAD Number | Name | Location |
|---|---|---|
| 41 | NC | |
| 42 | MS | [1677.700, 165.400] |
| 43 | CLK2 | [1799.600, 165.400] |
| 44 | CLK1 | [1921.500, 165.400] |
| 45 | NC | |
| 46 | FRM | [2043.400, 165.400] |
| 47 | M | [2165.300, 165.400] |
| 48 | NC | |
| 49 | PCCLK2 | [2275.300, 165.400] |
| 50 | DIO2 | [2397.200, 165.400] |
| 51 | NC | |
| 52 | CL2 | [2519.100, 165.400] |
| 53 | NC | |
| 54 | V0 | [2992.600, 98.200] |
| 55 | V5 | [2992.600, 222.200] |
| 56 | V4 | [2992.600, 346.200] |
| 57 | V1 | [2992.600, 470.200] |
| 58 | VEE | [2993.100, 608.400] |
| 59 | O64 | [2993.100, 718.400] |
| 60 | O63 | [2993.100, 828.400] |
| 61 | O62 | [2993.100, 938.400] |
| 62 | O61 | [2993.100, 1048.400] |
| 63 | O60 | [2993.100, 1158.400] |
| 64 | O59 | [2993.100, 1268.400] |
| 65 | O58 | [2993.100, 1378.400] |
| 66 | O57 | [2993.100, 1488.400] |
| 67 | O56 | [2993.100, 1598.400] |
| 68 | O55 | [2993.100, 1708.400] |
| 69 | O54 | [2993.100, 1818.400] |
| 70 | O53 | [2993.100, 1928.400] |
| 71 | O52 | [2993.100, 2038.400] |
| 72 | O51 | [2993.100, 2148.400] |
| 73 | O50 | [2993.100, 2258.400] |
| 74 | O49 | [2993.100, 2368.400] |
| 75 | O48 | [2993.100, 2478.400] |
| 76 | O47 | [2993.100, 2588.400] |
| 77 | O46 | [2993.100, 2698.400] |
| 78 | O45 | [2993.100, 2808.400] |
| 79 | O44 | [2993.100, 2918.400] |
| 80 | O43 | [2728.100, 2935.600] |
| 81 | O42 | [2618.100, 2935.600] |
| 82 | O41 | [2508.100, 2935.600] |
| 83 | O40 | [2398.100, 2935.600] |

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| PAD Number | Name | Location |
|---|---|---|
| 84 | O39 | [2288.100, 2935.600] |
| 85 | O38 | [2178.100, 2935.600] |
| 86 | O37 | [2068.100, 2935.600] |
| 87 | O36 | [1958.100, 2935.600] |
| 88 | O35 | [1848.100, 2935.600] |
| 89 | O34 | [1738.100, 2935.600] |
| 90 | O33 | [1628.100, 2935.600] |
| 91 | O32 | [1438.900, 2935.600] |
| 92 | O31 | [1328.900, 2935.600] |
| 93 | O30 | [1218.900, 2935.600] |
| 94 | O29 | [1108.900, 2935.600] |
| 95 | O28 | [998.900, 2935.600] |
| 96 | O27 | [888.900, 2935.600] |
| 97 | O26 | [778.900, 2935.600] |
| 98 | O25 | [668.900, 2935.600] |
| 99 | O24 | [558.900, 2935.600] |
| 100 | O23 | [448.900, 2935.600] |